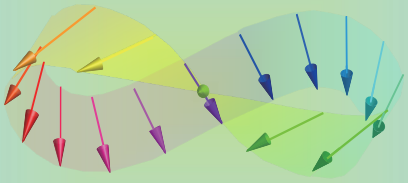
Information Storage and Spintronics 01



Atsufumi Hirohata

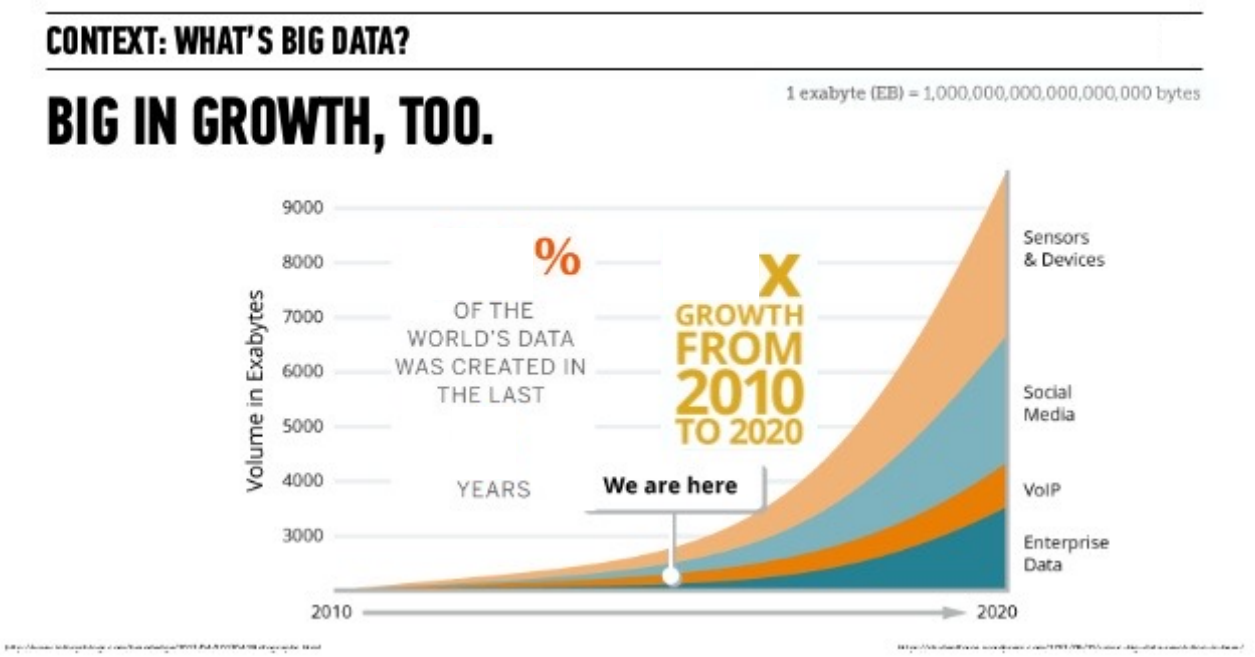
Department of Electronic Engineering

THE UNIVERSITY of York

14:00 Monday, 03/October/2022 (SLB 101)

Information Volume

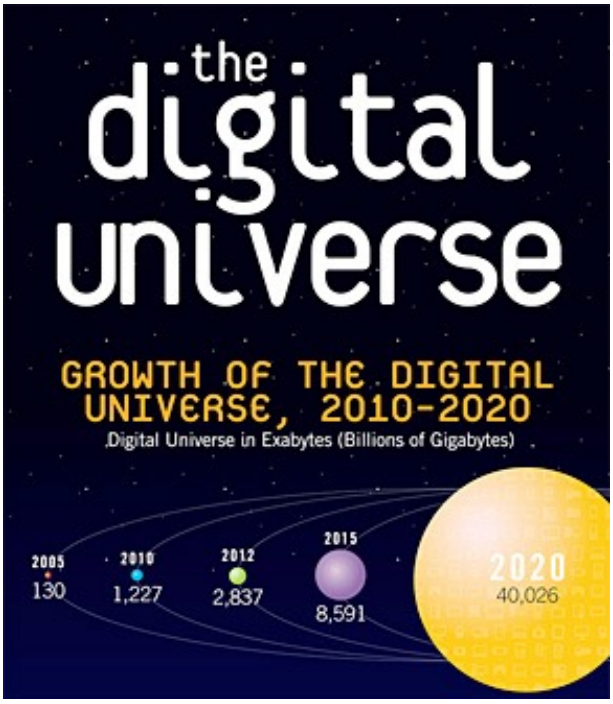
Information volume has been doubled every year : *



* https://avora.com/blog/rise-of-the-data-warehouse/

Digital Universe

Total digital information generated in the world : *



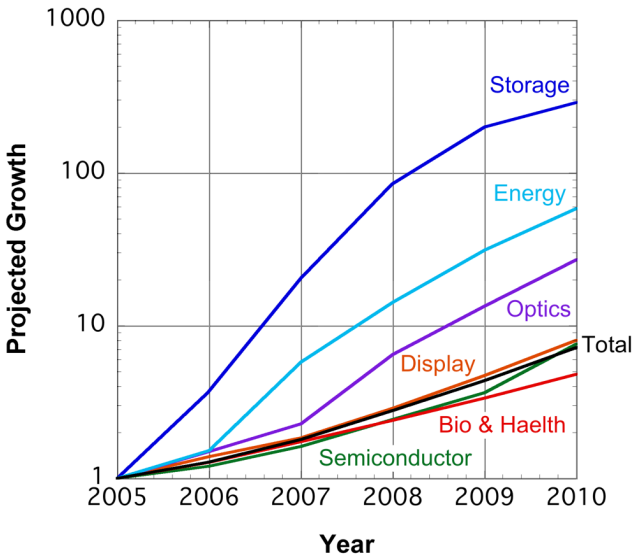
In 2012, 2.8 ZB (= 2.8×10^{21} B)

→ In 2020, 8.59 ZB (5.25 TB / person)

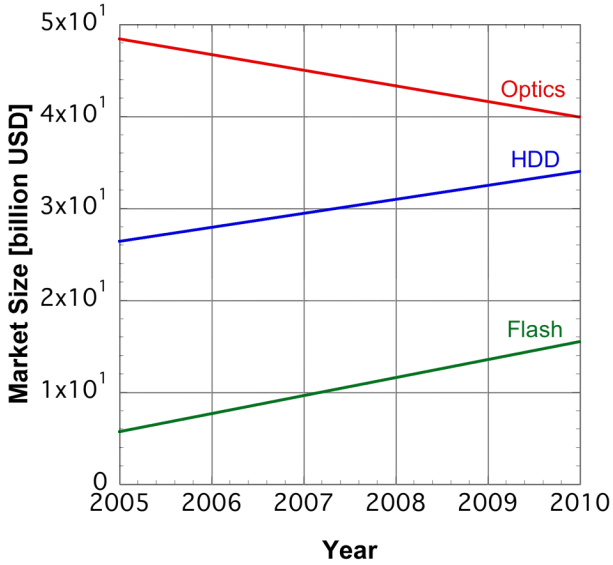
* IDC, The Diverse and Exploding Digital Universe 2020 (11 December 2012).

Potential Market Growth in Nanotechnology

Nanotechnology growth : *



Market size in major storage : **



* http://www.fuji-keizai.com/e/report/ww_nano_product_e.html;
** http://www.fcr.co.jp/; http://www.yano.co.jp/

Contents of Information Storage and Spintronics

Lectures : Atsufumi Hirohata (atsufumi.hirohata@york.ac.uk, P/Z 019)

Advancement in information storages and spintronics (Weeks 2 ~ 9)

All lectures will be uploaded weekly in advance at
http://www-users.york.ac.uk/~ah566/lectures/lectures.html

14:00 ~ 15:00 Mons. (SLB 101)

14:00 ~ 15:00 Thus. (SLB 101)

I. Introduction to information storage (01 & 02)

II. Magnetic information storages (03 ~ 06)

III. Solid-state information storages (07 ~ 11)

IV. Spintronic devices (12 ~ 18)

Practicals :

Analysis on a spintronic device using VSM, EDX, MFM and MR (Weeks 3 ~ 8)

Operation, data and instruction will be uploaded weekly in advance at
Internal Wiki page &
http://www-users.york.ac.uk/~ah566/lectures/lectures.html

13:00 ~ 15:00 Weds. (P/A 016, Nanocentre and P/Z 008)

Continuous Assessment :

Assignment to be submitted via VLE (Week 10).

References

Magnetic storages :

- S. X. Wang and A. M. Taratorin, *Magnetic Information Storage Technology* (Academic Press, New York, 1999).

- C. D. Mee and E. D. Daniel, *Magnetic Recording* (McGraw Hill, New York, 1996).

Semiconductor storages :

- D. Richter, *Flash Memories: Economic Principles of Performance, Cost and Reliability Optimization* (Springer, Berlin, 2013).

- J. Brewer and M. Gill, *Nonvolatile Memory Technologies with Emphasis on Flash: A Comprehensive Guide to Understanding and Using Flash Memory Devices* (Wiley-Blackwell, New York, 2008).

Spintronics :

- A. Hirohata and K. Takanashi, *J. Phys. D: Appl. Phys.* **47**, 193001 (2014).

- A. Hirohata *et al.*, *J. Magn. Magn. Mater.* **509**, 166711 (2020).

Lecture notes / slides : Internal Wiki page &
http://www-users.york.ac.uk/~ah566/lectures/lectures.html

01 Principles of Information Storage

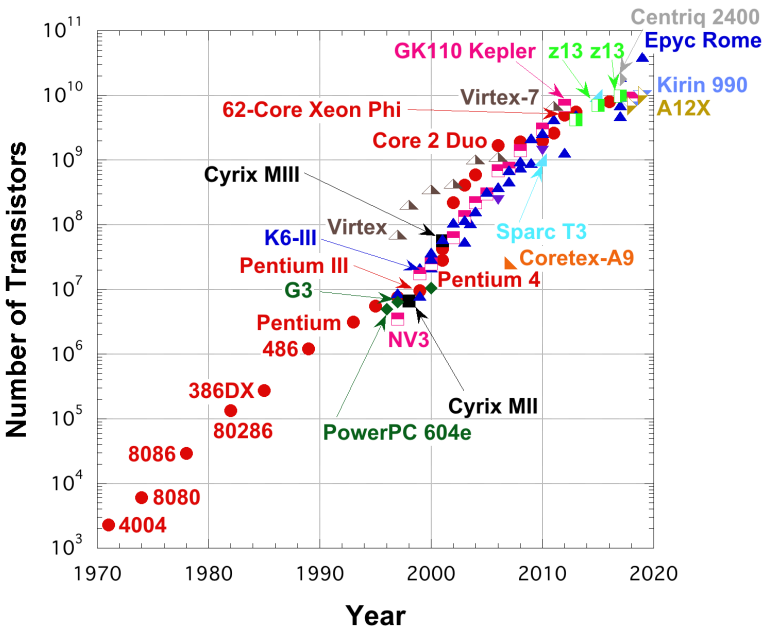
- Moore's law
- Information storage
- Von Neumann's model
- Internal connections
- Memory access
- Bit and byte

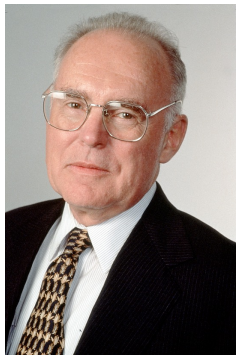
Miniaturisation and Integration in Semiconductor Devices

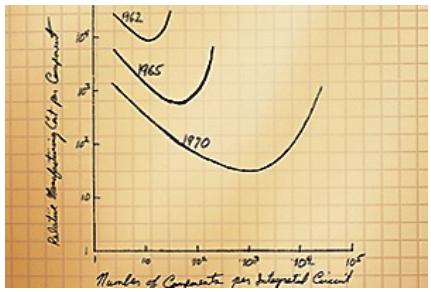
Moore's law : *

"The number of transistors on a chip will double every months." (1965)

10 years later he revised this to "every months."





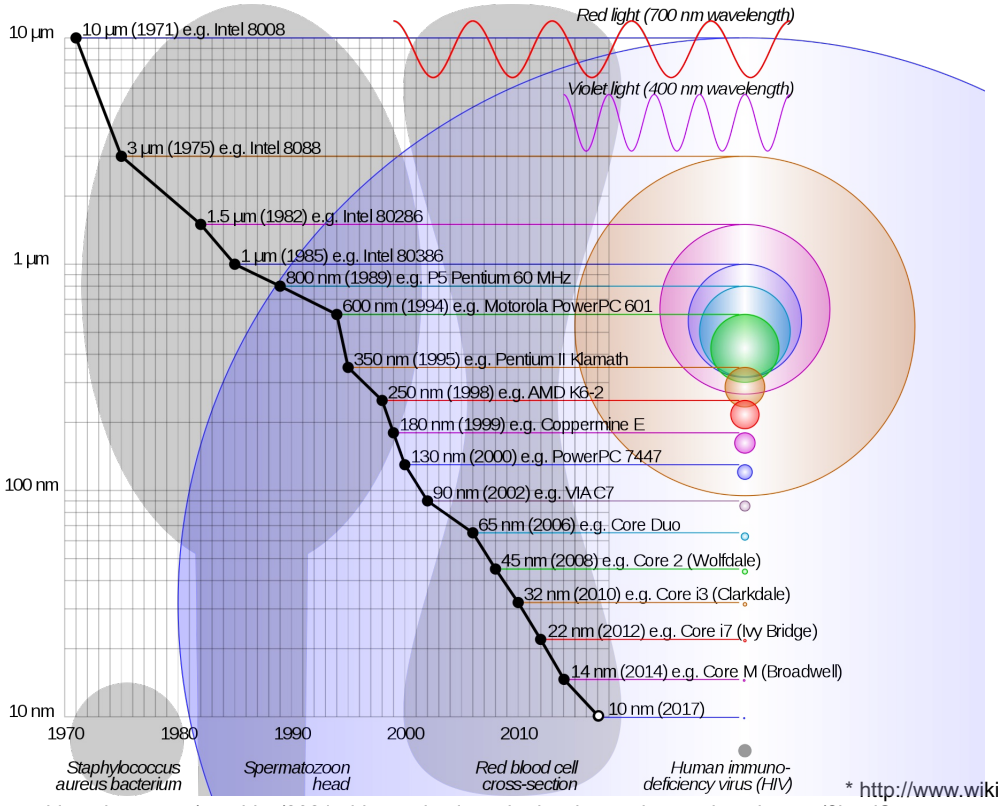


→ The development speed becomes even faster !

* http://www.intel.com/

Fabrication Technology for Semiconductor Devices

Fabrication rules and technology : *



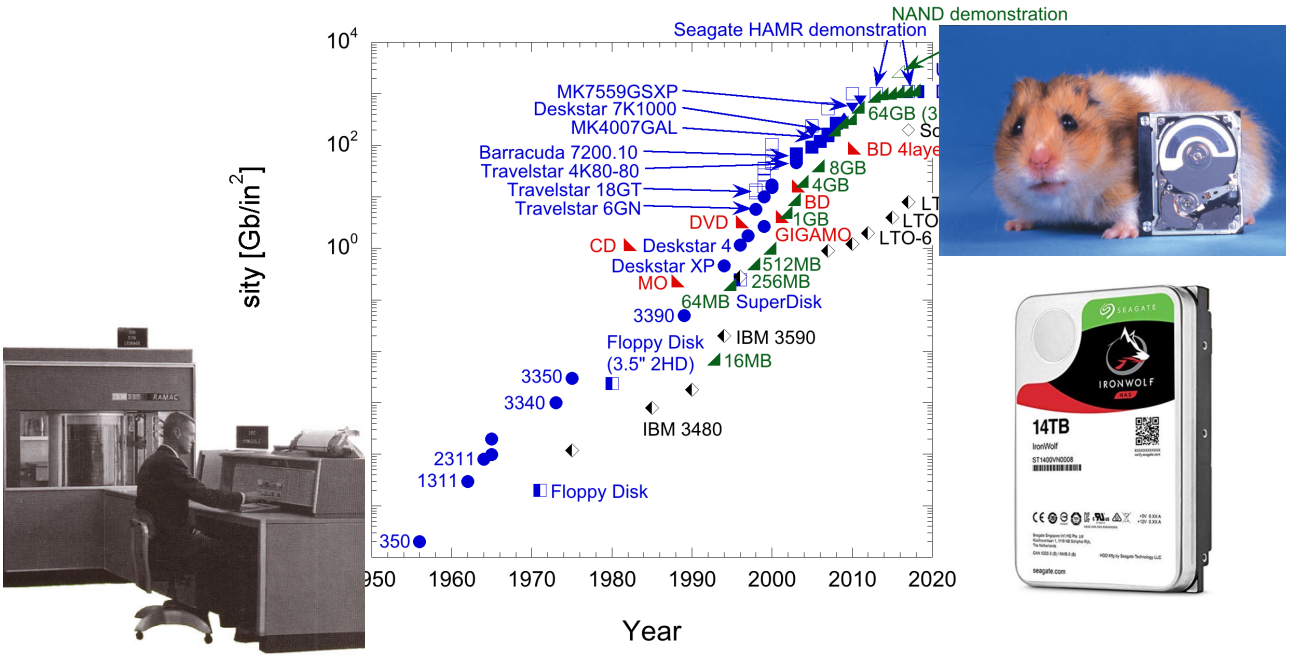
* http://www.wikipedia.org;
https://www.bloomberg.com/graphics/2021-chip-production-why-hard-to-make-semiconductors/?leadSource=uverify%20wall

Increase in Recording Density of Hard Disc Drives

Similar to Moore's law :

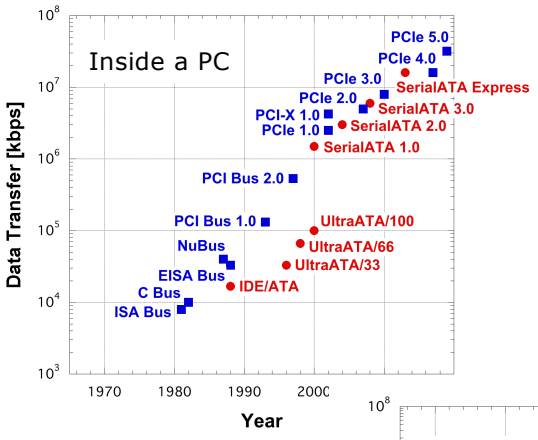
Areal density in a hard disc drive (HDD) doubles every months. (~ 1992)

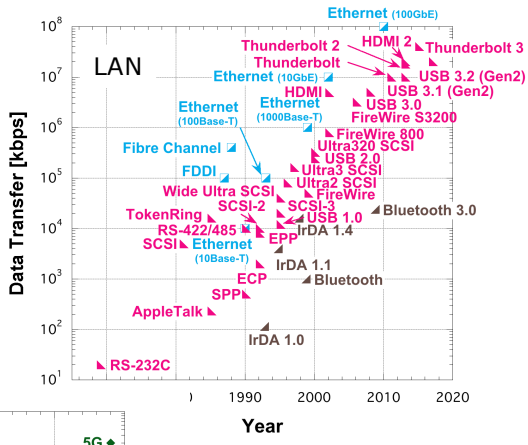
After giant magnetoresistance (GMR) implementation,
it doubles less than every months. (1992 ~)

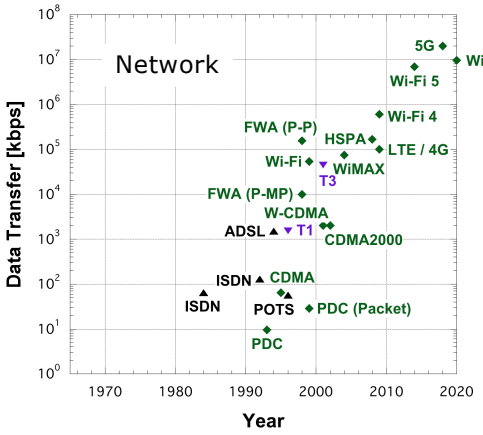


Advancement in Communication Technologies

Similar to Moore's law : Data transfer becomes faster.

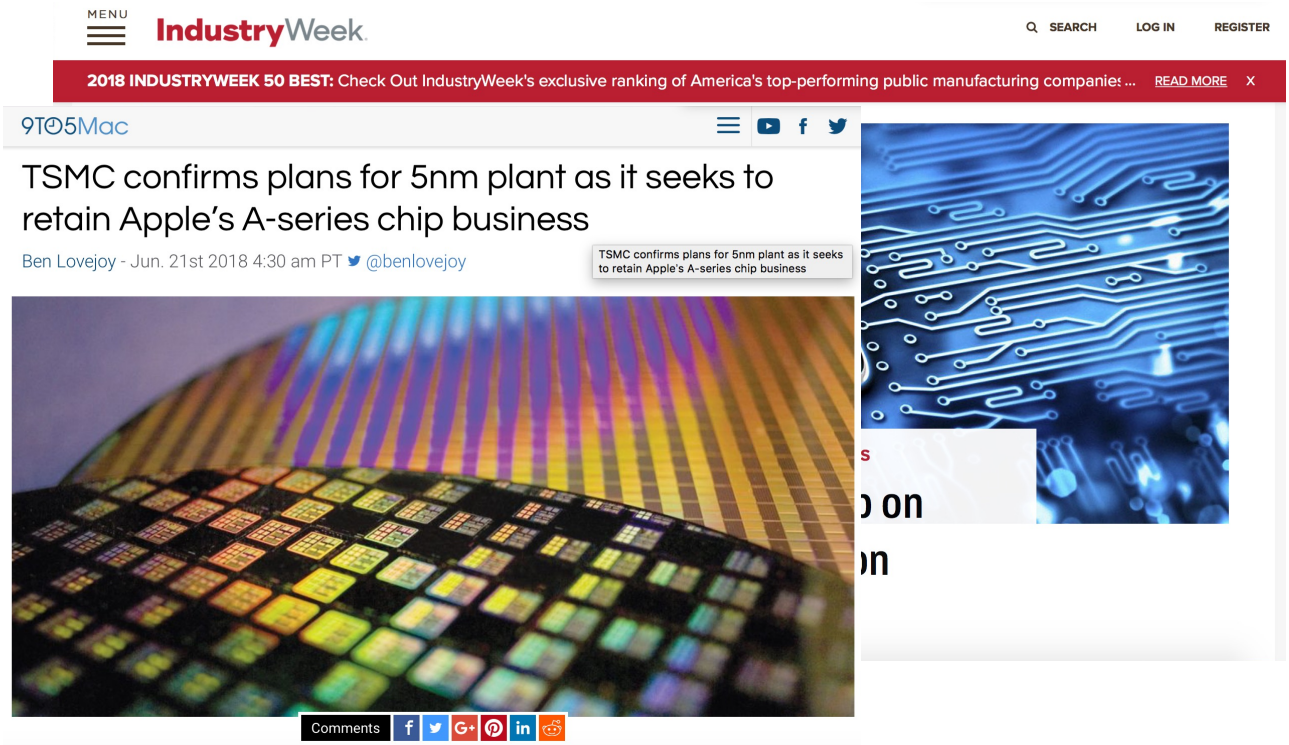






Can We Continue Such Trends ?

Further miniaturisation is too expensive :

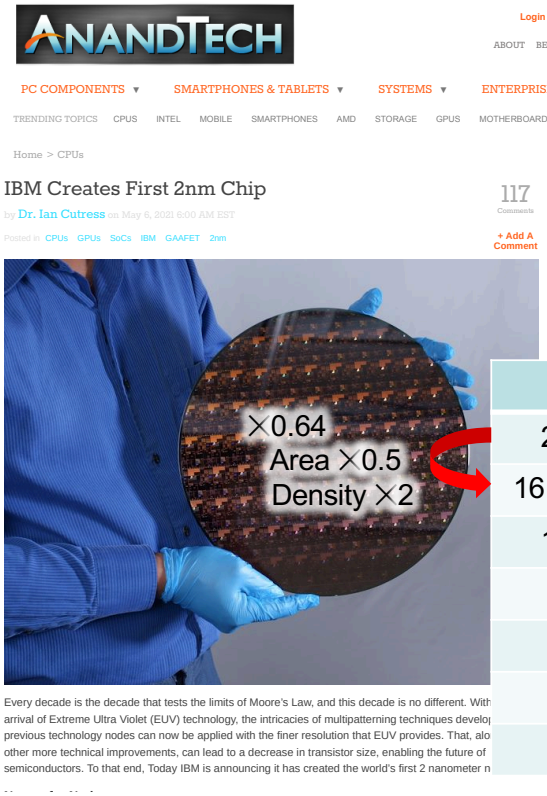


* https://www.industryweek.com/emerging-technologies/globalfoundries-gives-advanced-chip-production-technology

** https://9to5mac.com/2018/06/21/tsmc-5nm-process-plant/amp/

Latest 2 nm Fabrication Rule

In 2021, IBM announced the first demonstration of 2-nm-ruled chip : *



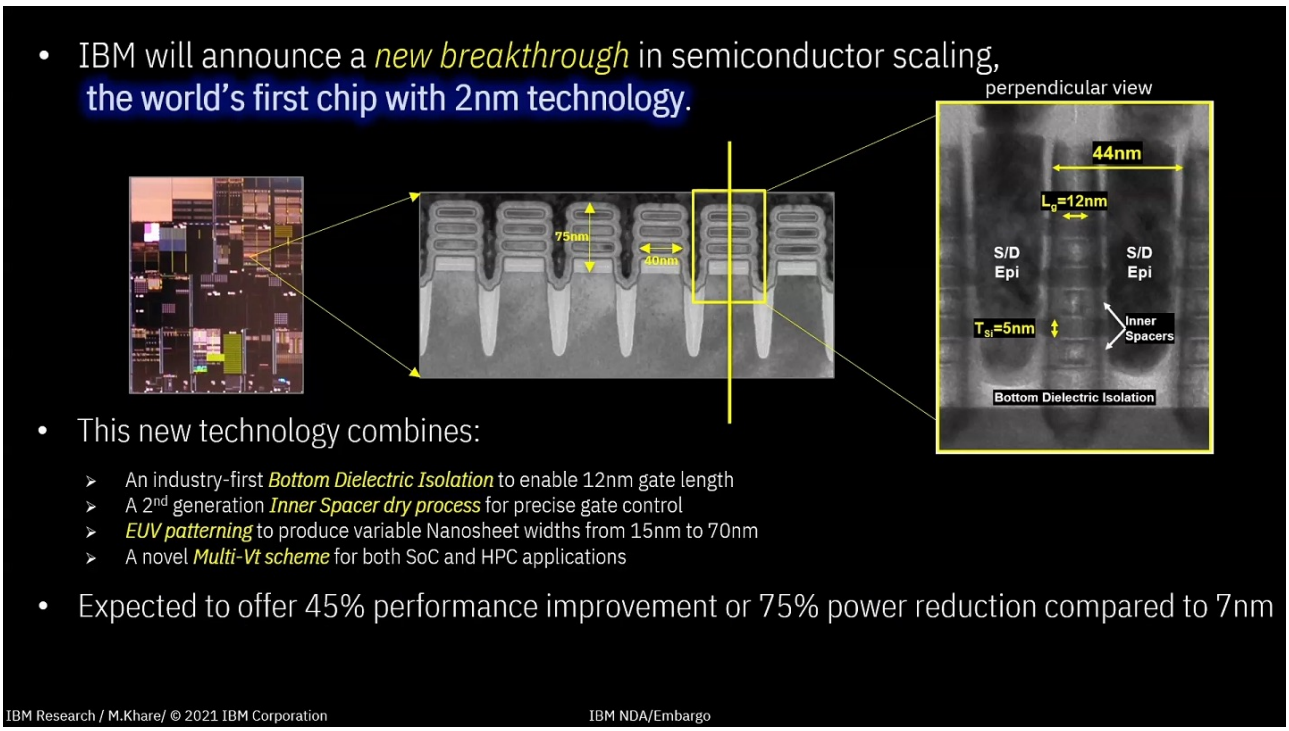
Peak Quoted Transistor Densities [MTr/mm^2]

	IBM	TSMC	Intel	Samsung
22 nm			16.50	
16 / 14 nm		28.88	44.67	33.32
10 nm		52.51	100.76	51.82
7 nm		91.20	237.18	95.08
5 nm		171.30		
3 nm		292.21		
2 nm	333.33			

* https://www.anandtech.com/show/16656/ibm-creates-first-2nm-chip

Latest 2 nm Fabrication Rule

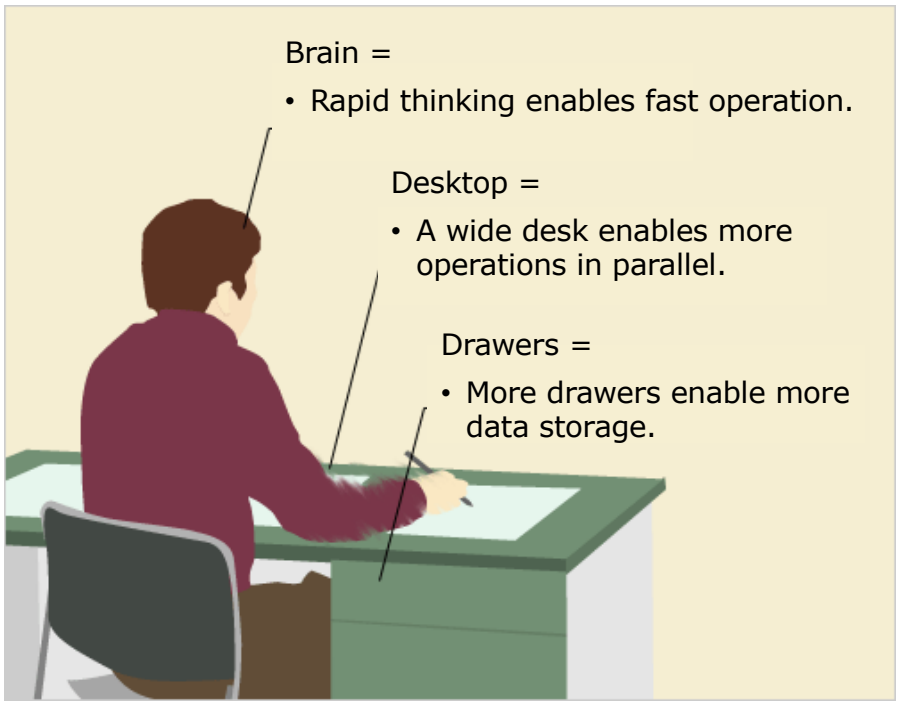
In 2021, IBM announced the first demonstration of 2-nm-ruled chip : *



* https://www.anandtech.com/show/16656/ibm-creates-first-2nm-chip

Information Storage ?

Analogue to our life : *



* http://support.nifty.com/tsushin/cs/column/detail/090831543366/1.htm

Information Technology Pyramid

Layered structures between CPU and storages : *

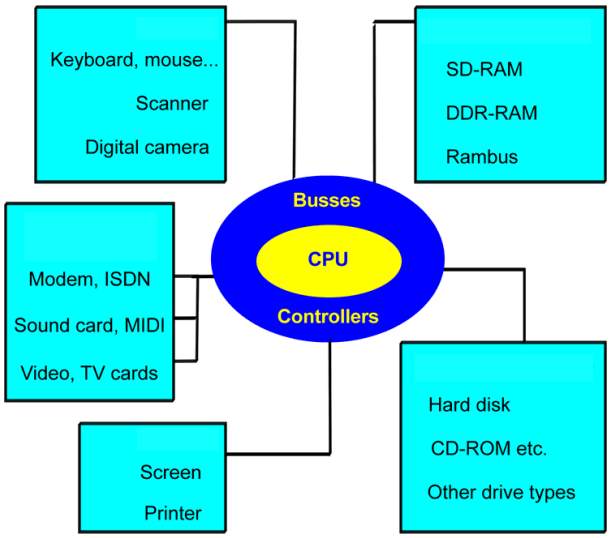
* http://www.howstuffworks.com/computer-memory1.htm

Von Neumann's Model

In 1940s, John von Neumann developed a basic model for a computer. *

Von Neumann categorised into 5 key components :

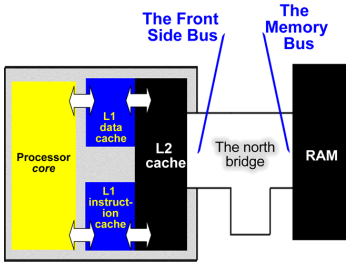
- CPU
- Input
- Output
- Working storage
- Permanent storage

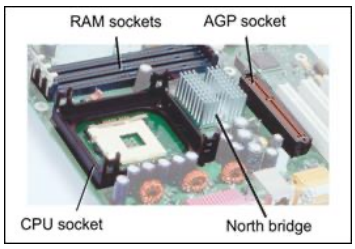


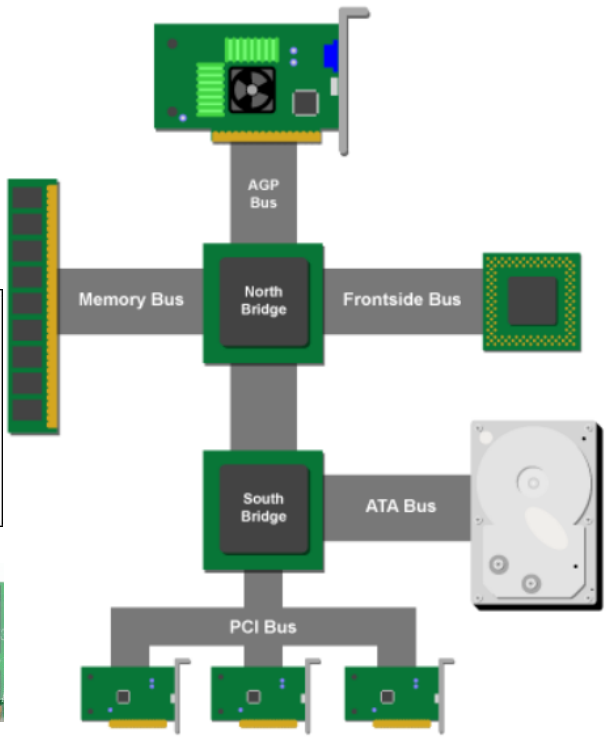
* http://karbosguide.com/books/pcarchitecture/chapter02.htm

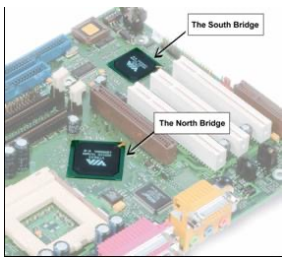
Connections between the Components

Connections between CPU, in/outputs and storages :





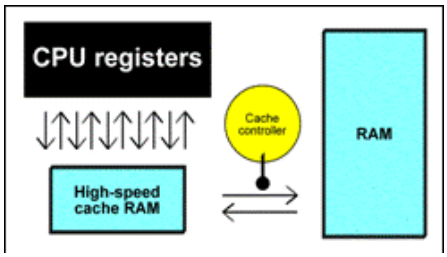


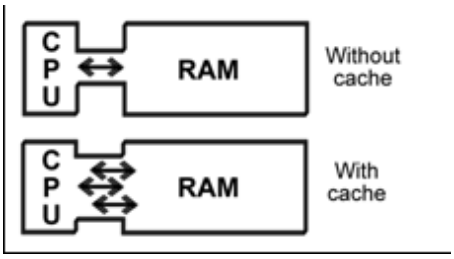


* http://testbench.in/introduction_to_pci_express.html;
** http://karbosguide.com/books/pcarchitecture/chapter06.htm

How Does a CPU Work ?

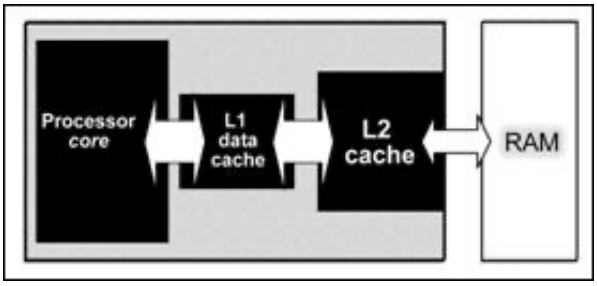
Data transfer between CPU and working storage : *





A 32-bit CPU can handle data in different sized packets :

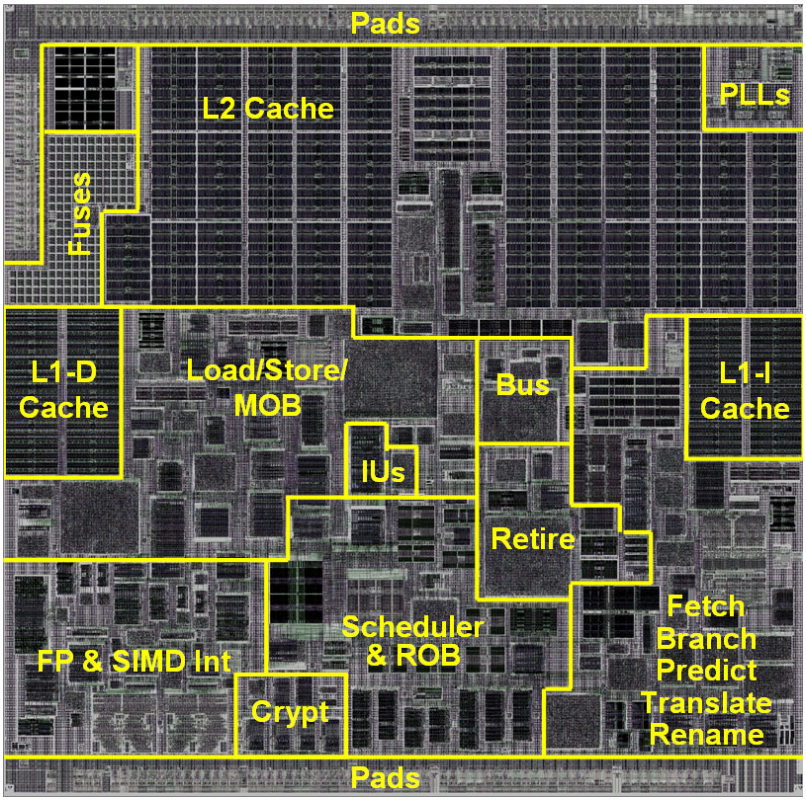
- *bytes* (bits)
- *half-words* (bits)
- *words* (bits)
- *blocks* (larger groups of bits)



* http://karbosguide.com/books/pcarchitecture/chapter10.htm

CPU Architecture

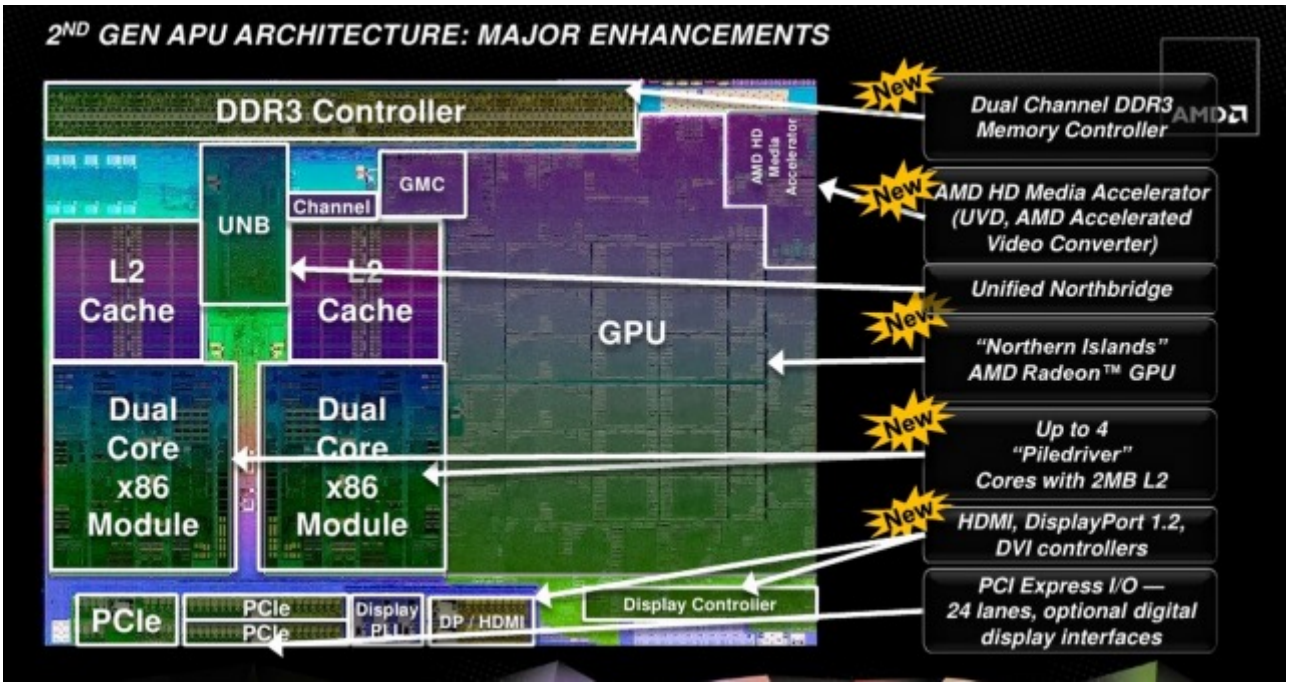
For example, VIA Nano processor : *



* http://www.xbitlabs.com/articles/cpu/display/intelatom-vianano_3.html

CPU Architecture

Recent development by AMD, Trinity CPU / GPU architecture : *



* https://arstechnica.com/information-technology/2012/05/amd-ships-trinity-processor-aims-for-a-piece-of-intels-ultrabook-market/

Instruction Set Architecture for CPU

Assembly language :

CPU can only handle :

- Binary code

Mnemonic :

- ADD / SUB etc.

Number of syntax :

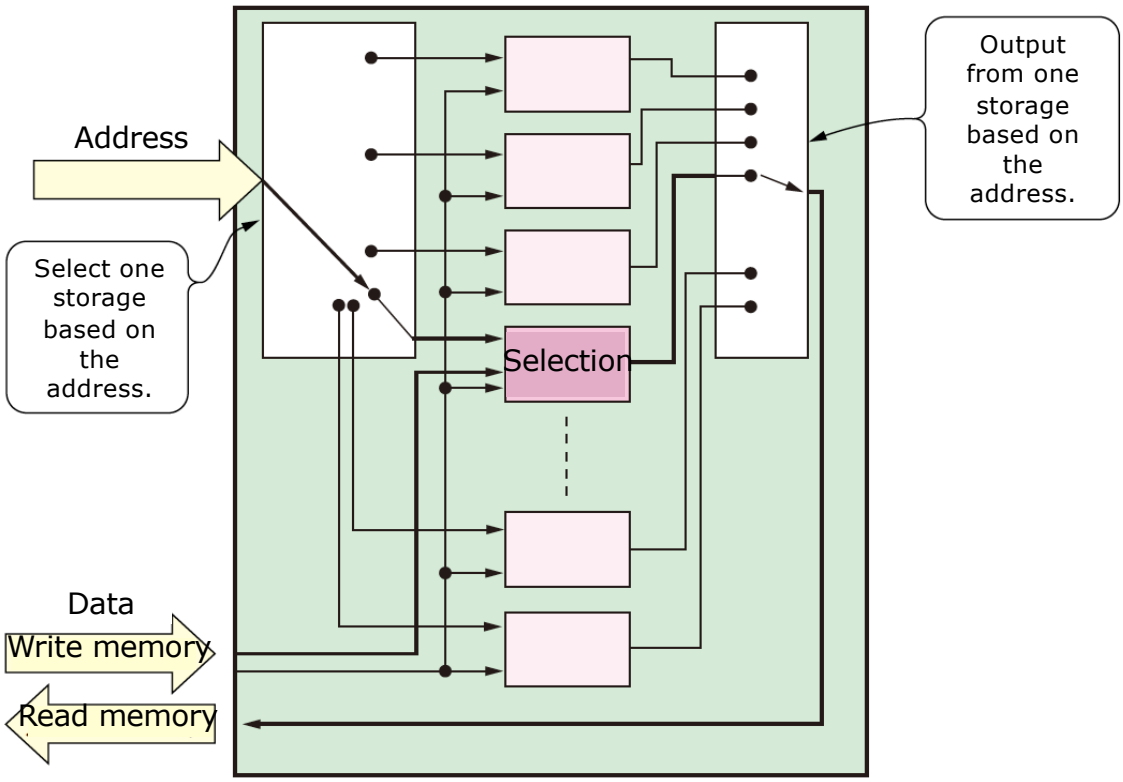
- Typically 100 ~ 200
- Maximum ~ 400

```
MONITOR FOR 6802 1.4          9-14-80  TSC ASSEMBLER  PAGE    2


 C000                   ORG    ROM+$0000 BEGIN MONITOR
 C000 8E 00 70  START   LDS    #STACK

                ****************************************
                * FUNCTION: INITA - Initialize ACIA
                * INPUT: none
                * OUTPUT: none
                * CALLS: none
                * DESTROYS: acc A

 0013           RESETA  EQU    %00010011
 0011           CTLREG  EQU    %00010001

 C003 86 13     INITA   LDA A  #RESETA   RESET ACIA
 C005 B7 80 04          STA A  ACIA
 C008 86 11             LDA A  #CTLREG   SET 8 BITS AND 2 STOP
 C00A B7 80 04          STA A  ACIA

 C00D 7E C0 F1          JMP    SIGNON    GO TO START OF MONITOR

                ****************************************
                * FUNCTION: INCH - Input character
                * INPUT: none
                * OUTPUT: char in acc A
                * DESTROYS: acc A
                * CALLS: none
                * DESCRIPTION: Gets 1 character from terminal

 C010 B6 80 04  INCH    LDA A  ACIA      GET STATUS
 C013 47                ASR A            SHIFT RDRF FLAG INTO CARRY
 C014 24 FA             BCC    INCH      RECIEVE NOT READY
 C016 B6 80 05          LDA A  ACIA+1    GET CHAR
 C019 84 7F             AND A  #$7F      MASK PARITY
 C01B 7E C0 79          JMP    OUTCH     ECHO & RTS

                ****************************************
                * FUNCTION: INHEX - INPUT HEX DIGIT
                * INPUT: none
                * OUTPUT: Digit in acc A
                * CALLS: INCH
                * DESTROYS: acc A
                * Returns to monitor if not HEX input

 C01E 8D F0     INHEX   BSR    INCH      GET A CHAR
 C020 81 30             CMP A  #'0       ZERO
 C022 2B 11             BMI    HEXERR    NOT HEX
 C024 81 39             CMP A  #'9       NINE
 C026 2F 0A             BLE    HEXRTS    GOOD HEX
 C028 81 41             CMP A  #'A
 C02A 2B 09             BMI    HEXERR    NOT HEX
 C02C 81 46             CMP A  #'F
 C02E 2E 05             BGT    HEXERR
 C030 80 07             SUB A  #7        FIX A-F
 C032 84 0F     HEXRTS  AND A  #$0F      CONVERT ASCII TO DIGIT
 C034 39                RTS

 C035 7E C0 AF  HEXERR  JMP    CTRL      RETURN TO CONTROL LOOP
```

* http://www.wikipedia.org/

Memory Access

In principle, only the CPU can (re-)write memory contents : *



* A. Nalamori, *Interface* **Feb.**, 44 (2006).

Read Memory

In a 32-bit CPU, the address is typically 32-bit integer : *

0x00000000 ~ 0xFFFFFFFF

= 4,294,967,296 = 4G

Address :

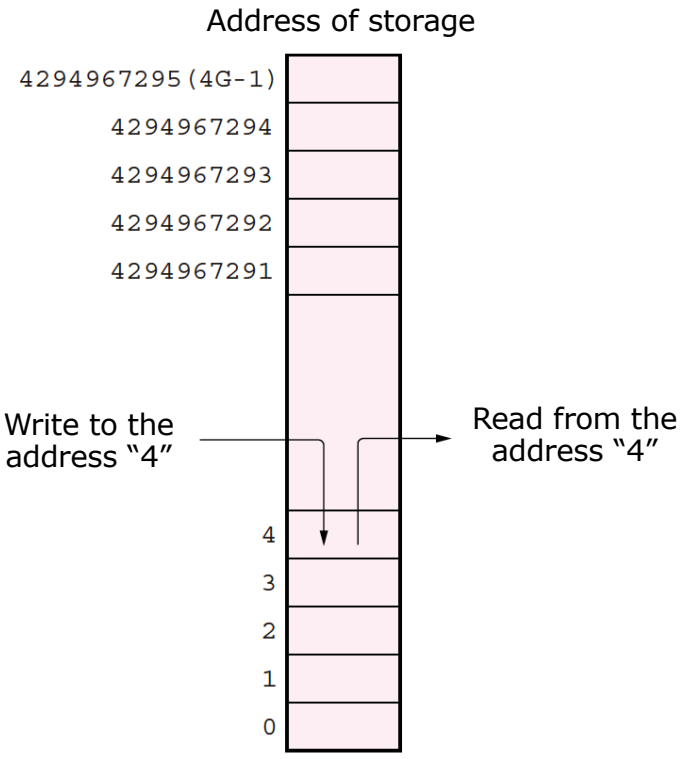
32-bit integer data

= Byte (1 Byte = bit)

= addresses to be stored

Read 32-bit integer data

Read four 4 Byte data from the addresses of a, (a+1), (a+2), (a+3) and construct them into one data.



* A. Nalamori, *Interface* **Feb.**, 44 (2006).

Write Memory

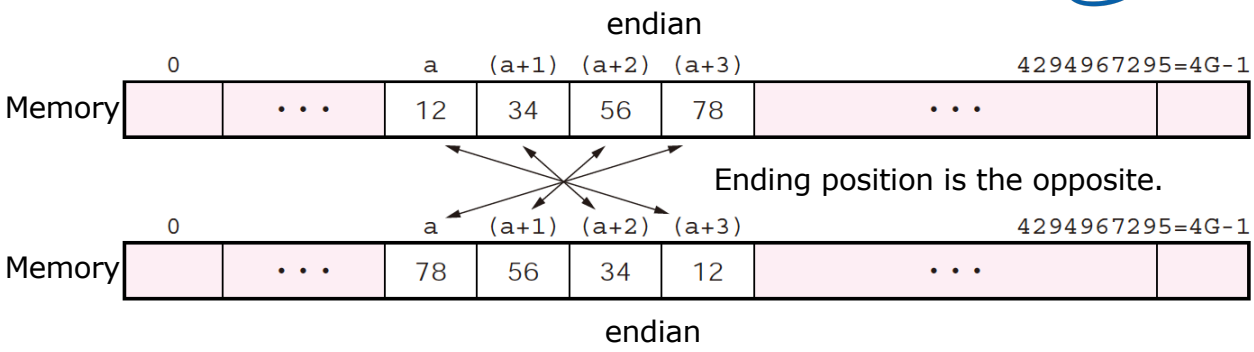
For example, write 32-bit integer data of "0x12345678" : *

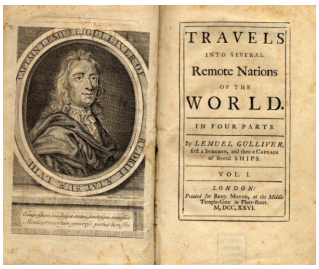
8-bit data : 0x12, 0x34, 0x56, 0x78

To store these data

Most significant bit is stored at the lowest address. → endian

Least significant bit is stored at the lowest address. → endian



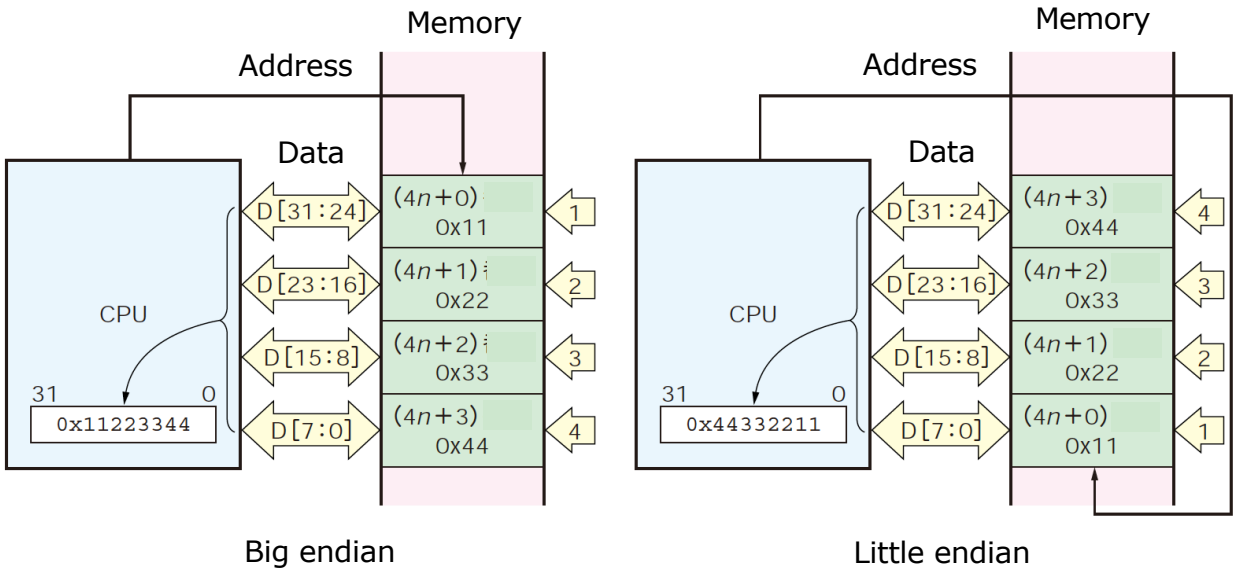


These are named after *"Gulliver's Travels"*.

* A. Nalamori, *Interface* **Feb.**, 44 (2006);
** http://www.wikipedia.org/

Memory Access for Big / Little Endian

Data bus holds the same data :



Nowadays most CPU can handle both endianness.

→ endian

* A. Nalamori, *Interface* **Feb.**, 44 (2006).

Bit and Byte

Bit :

"Binary digit" is a basic data size in information storage.

1 bit : 2 = combinations ; digit in binary number

2 2 =

3 2 =

4 2 =

: : : :

Byte :

A data unit to represent one letter in Latin character set.

1 byte (B) = bit

1 kB = 1 B ×

1 MB = 1 kB ×

: :