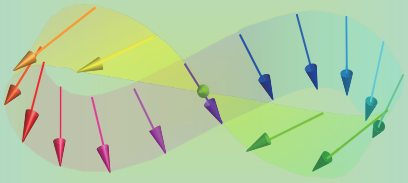
Information Storage and Spintronics 09



Atsufumi Hirohata

Department of Electronic Engineering

THE UNIVERSITY of York

14:00 Thursday, 27/October/2022 (SLB 101)

Quick Review over the Last Lecture

Flash memory :

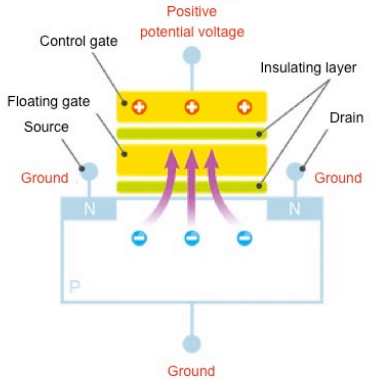
NOR-type

- ✓ high-speed read-out
- × writing speed
- × to integrate

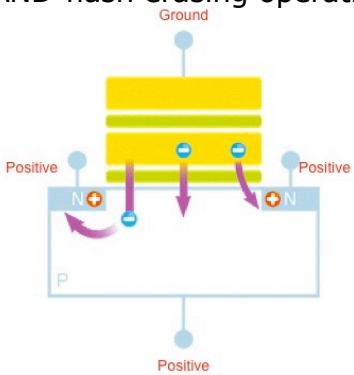
NAND-type

- × byte high-speed read-out
- ✓ writing speed
- ✓ for integration
- × Flash erase for a only !

NAND-flash writing operation :



NAND-flash erasing operation :



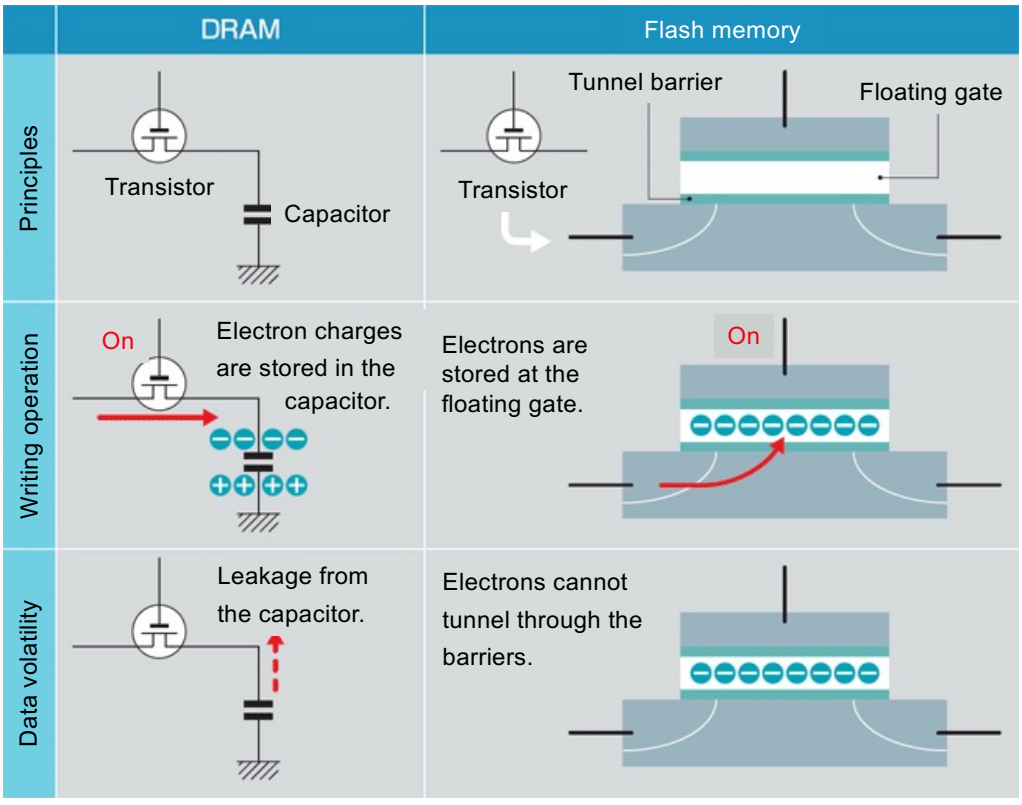
* http://www.tdk.co.jp/techmag/knowledge/200705/index2.htm

09 Dynamic Random Access Memory

- Memory cell
- Architecture
- Data storage
- Read-out
- Refresh
- Further integration

Flash Memory vs DRAM

Comparisons between flash memory and DRAM :



* http://pc.nikkeibp.co.jp/article/NPC/20061228/257976/

Storage and Working Memories

Current major memories for storage and work :

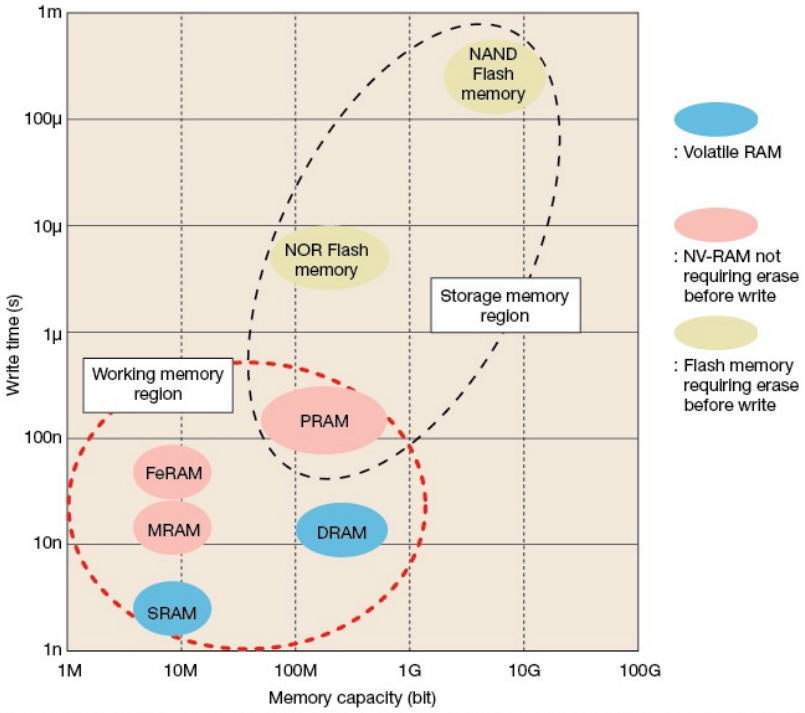
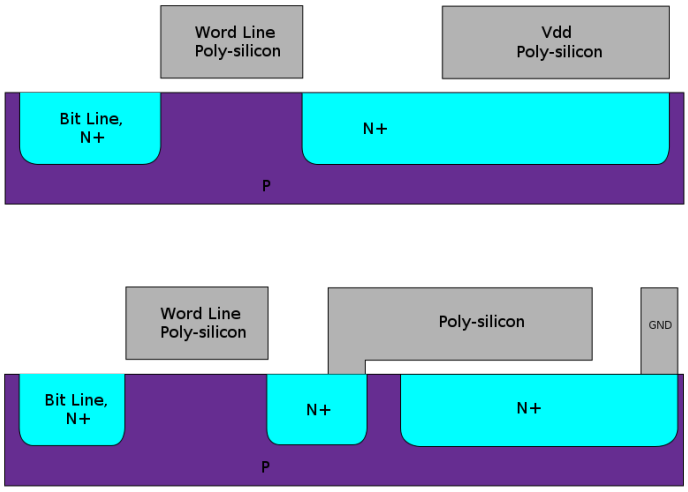


Fig 1 Host of New Non-Volatile RAMs Offer Fast Write, No Data Loss Diagram shows a comparison by write time and memory capacity. NOR Flash memory write time is per-byte, and NAND Flash memory per-page.

* http://techon.nikkeibp.co.jp/article/HONSHI/20070926/139715/

Dynamic Random Access Memory (DRAM)

In a computer, data is transferred from a HDD to a Dynamic Random Access Memory :



Data stored in a capacitor.

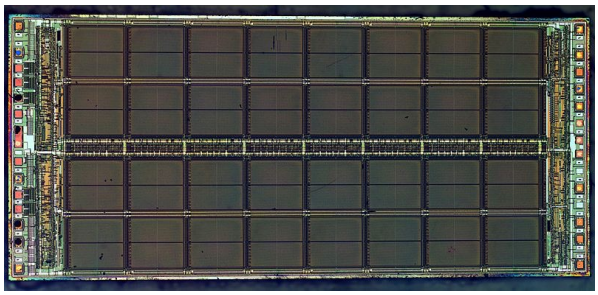
→ Electric charge needs to be .

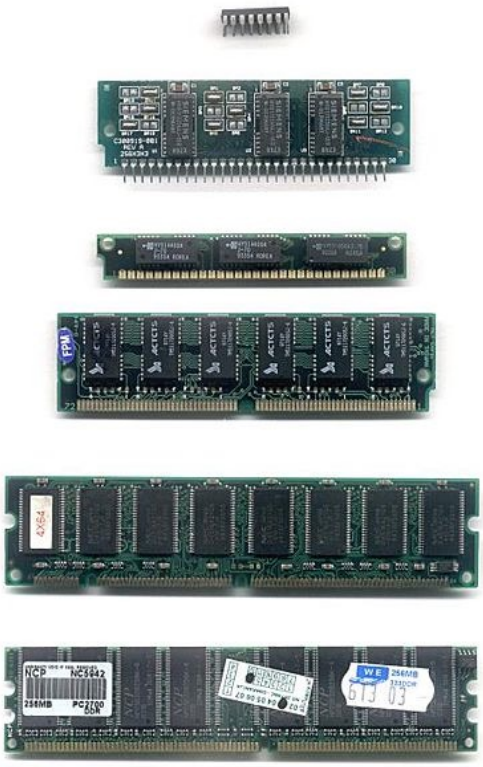
→ DRAM requires .

* http://www.wikipedia.org/

DRAM Packages

DRAM design :





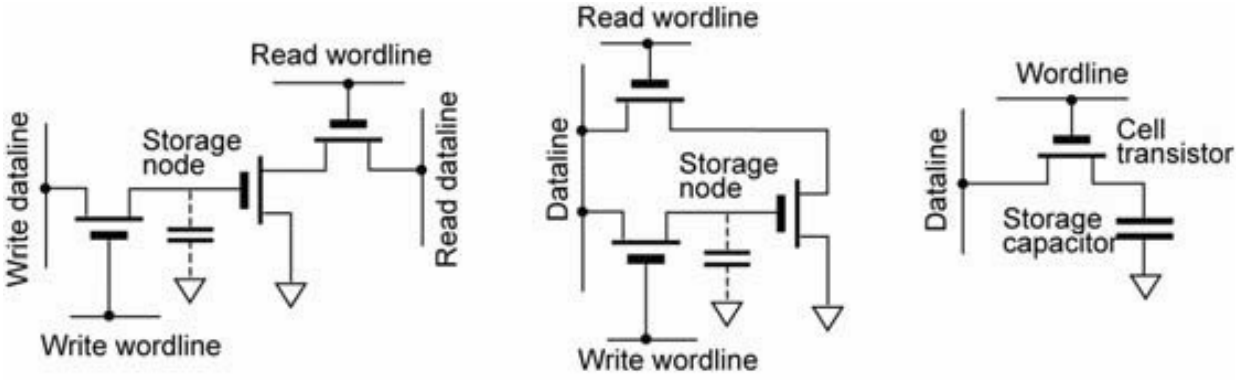
DRAM packages :

- Dual in-line package (DIP)
- Single in-line pin package (SIPP)
- Single in-line memory module (SIMM) 30-pin
- SIMM 72-pin
- Dual in-line memory module (DIMM) 168-pin
- Double data rate (DDR) DIMM 184-pin

* http://www.wikipedia.org/

Memory Cell Development

DRAM memory cells :



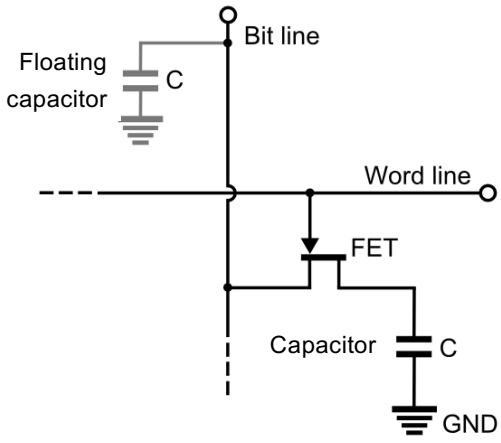
* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/dimension-increase-in-metal-oxide-semiconductor-memories-and-transistors

DRAM Operation

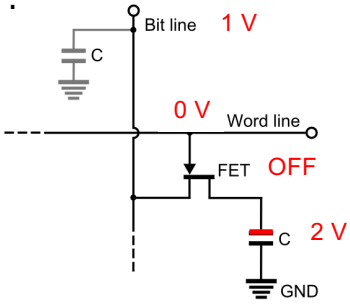
* https://www.youtube.com/watch?v=Lozf9sceW_o

Memory Storage

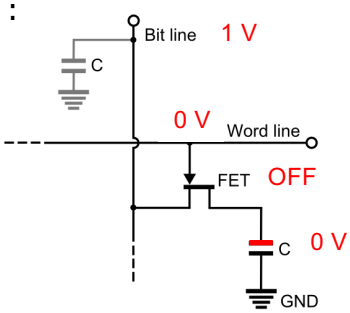
1 DRAM cell consists of 1 capacitor + 1 switching FET (1C1T) :



"1"-state :



"0"-state :

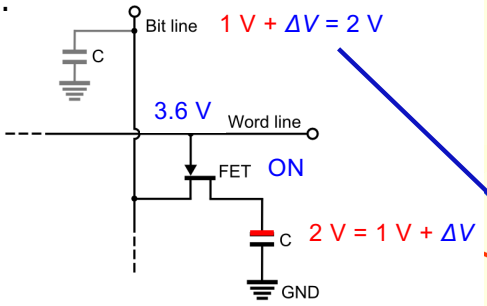


* http://www.wikipedia.org/

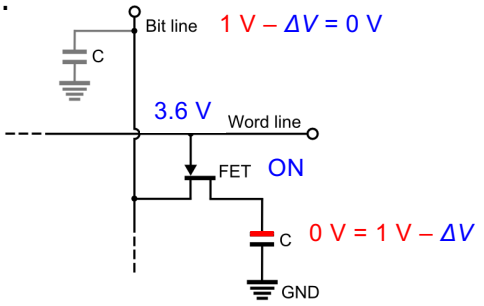
Memory Read-Out

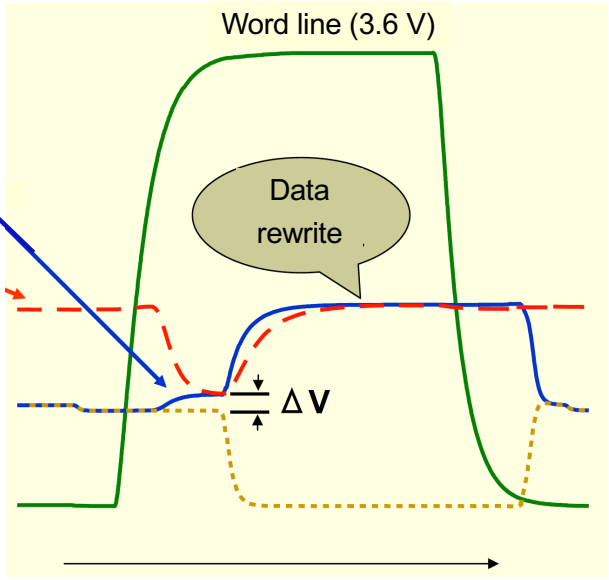
Read-out operation of 1C1T :

"1"-data :



"0"-data :

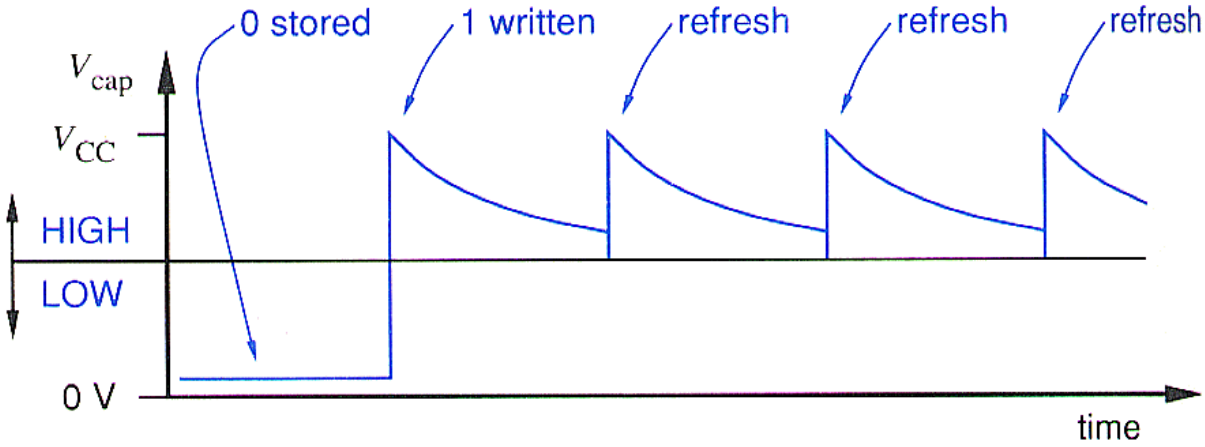




* http://www.wikipedia.org/;
** http://www.ritsumei.ac.jp/se/re/fujinolab/IntroLSI/IntroLSI-11.pdf

Memory Refresh

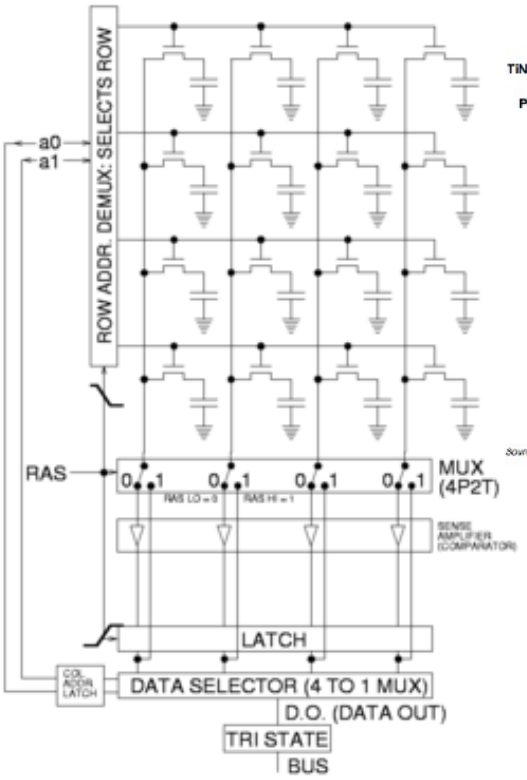
Refresh operation of 1C1T :

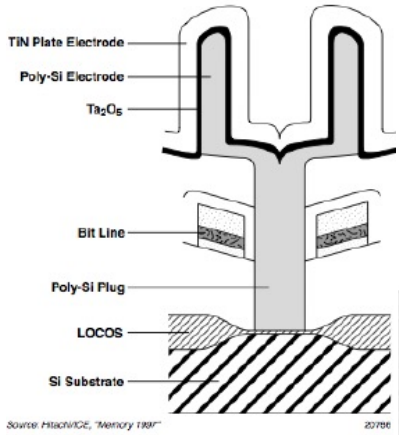


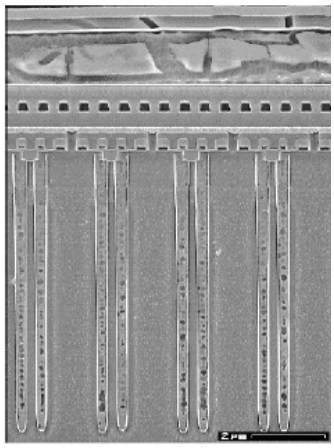
* http://users.cis.fiu.edu/~prabakar/cda4101/Common/notes/lecture09.html

DRAM Architecture

DRAM architecture :







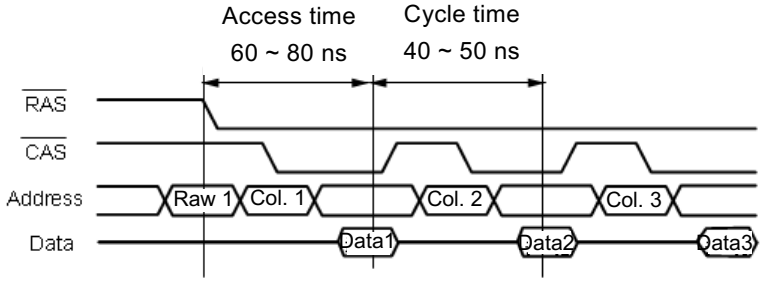
* http://www.wikipedia.org/
** https://cseweb.ucsd.edu/classes/fa11/cse240A-a/Slides1/02_Technology-2.pdf

Data Access Speed

Addressing a cell :

- Raw address strobe (RAS)
- Column address strobe (CAS)
- Page mode enables to address different columns in the same raw.

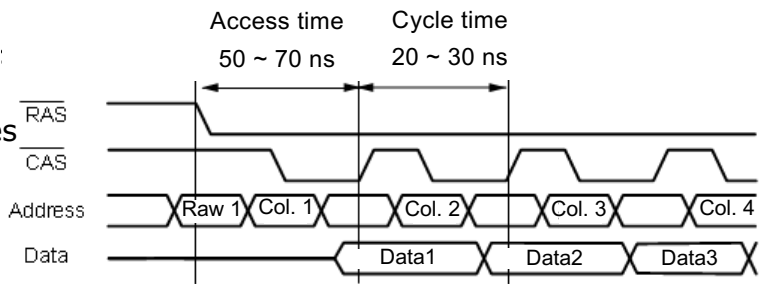
→ page mode



→

→ Synchronous DRAM

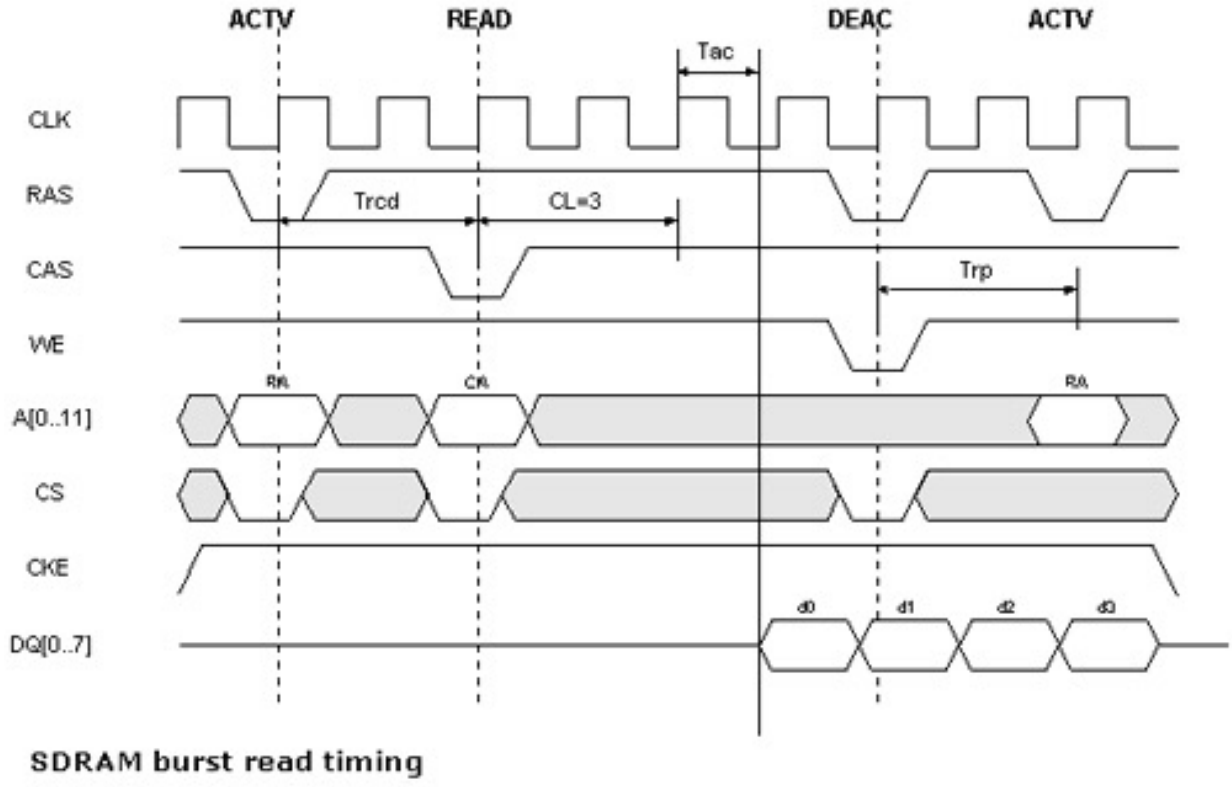
PC-100 : 100 MHz cycles



* http://www.elsena.co.jp/elspear/specialist_column/ddr-sdram.html

Synchronous DRAM (SDRAM)

SDRAM access diagram :

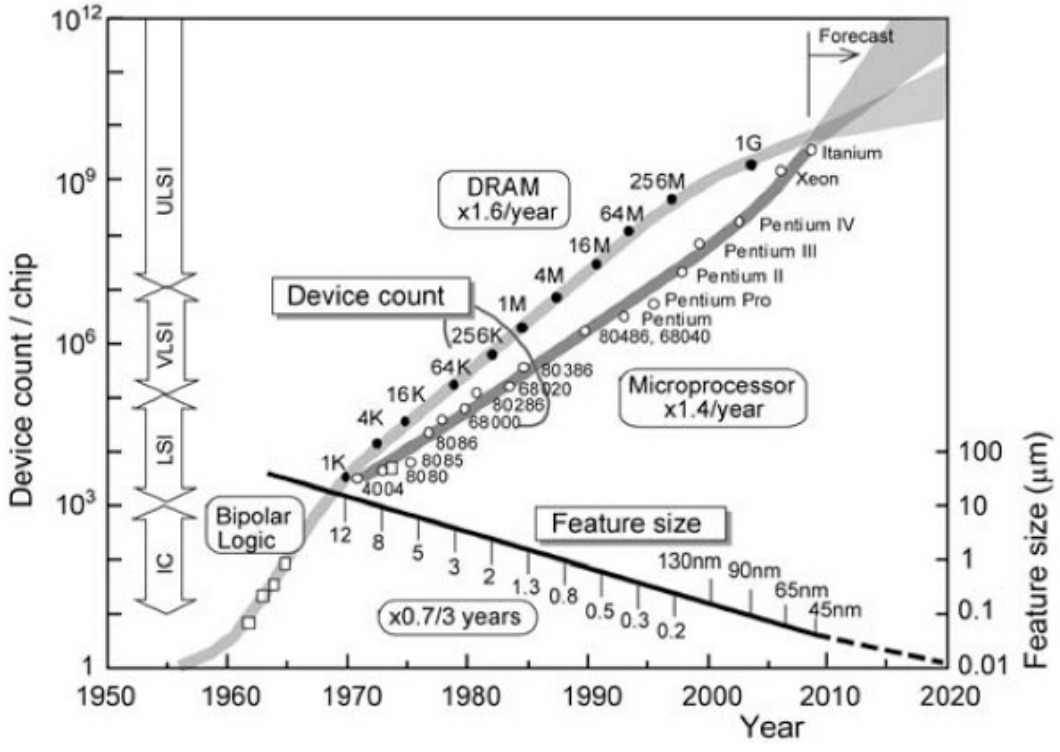


SDRAM burst read timing

* http://www.dewassoc.com/performance/memory/memory_speeds.htm

DRAM Trends

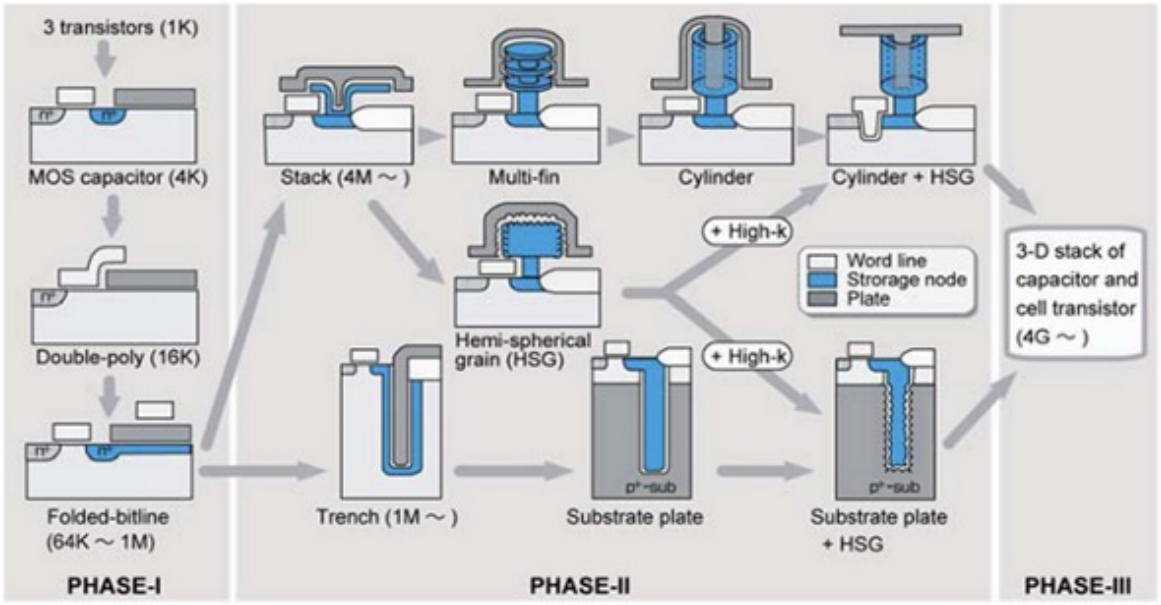
DRAM follows Moore's law (160 % / yr.) :



* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/dimension-increase-in-metal-oxide-semiconductor-memories-and-transistors

DRAM Design Developments

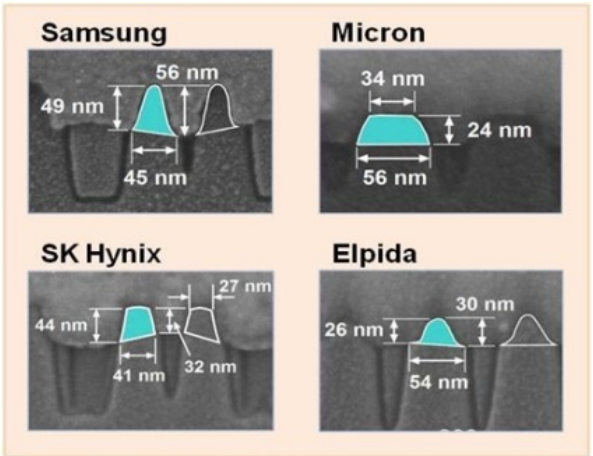
Storage node shapes :

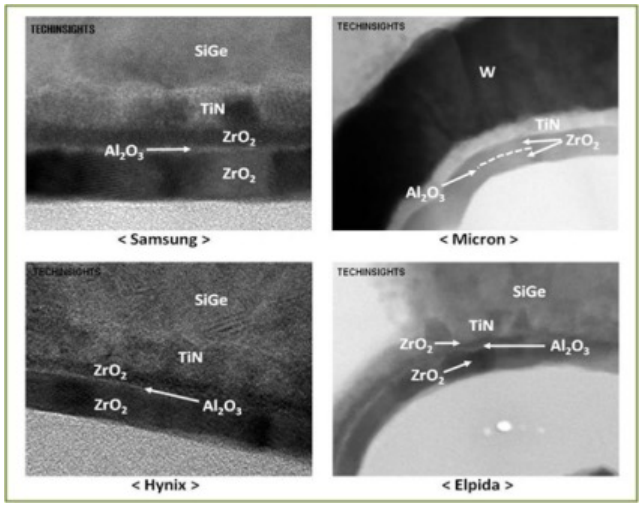


* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/dimension-increase-in-metal-oxide-semiconductor-memories-and-transistors

Fin-Type DRAM Designs

Various manufacturers developed different designs :

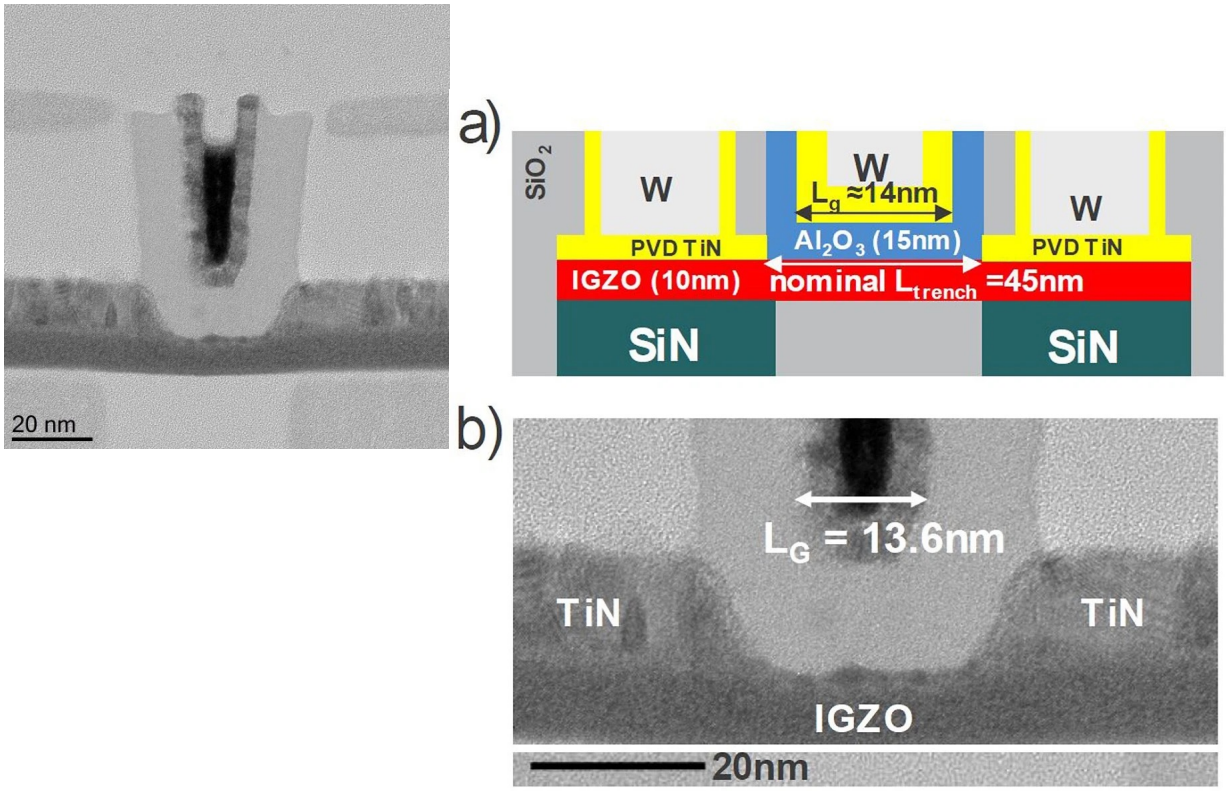




* http://eetimes.jp/ee/articles/1306/14/news072.html

DRAM with IGZO

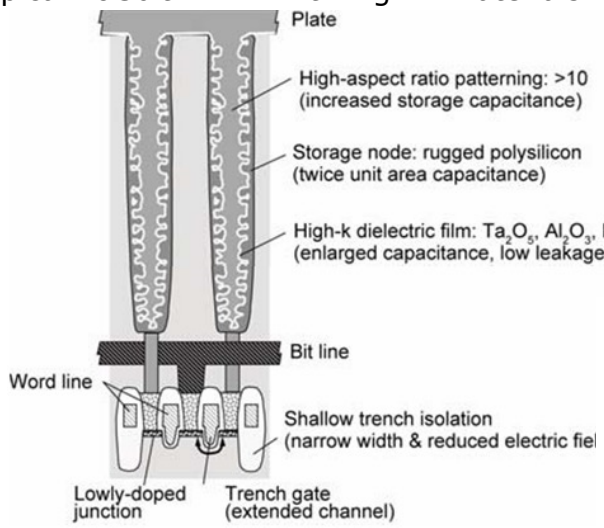
Various manufacturers developed different designs :

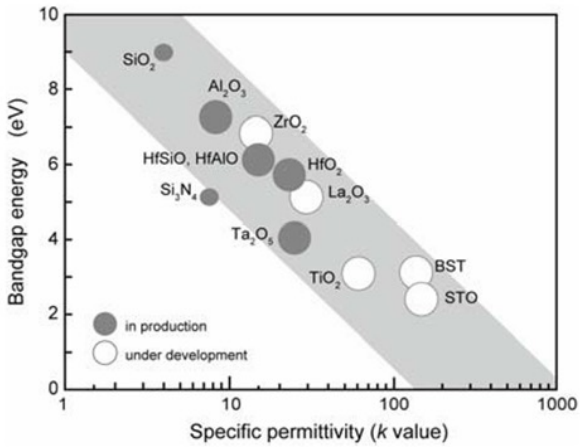


* https://www.eetimes.eu/capacitorless-dram-cell-on-igzo-base-shows-promising-values/

Cells, Pages and Blocks

Typical 10Gbit DRAM with high-*k* materials :



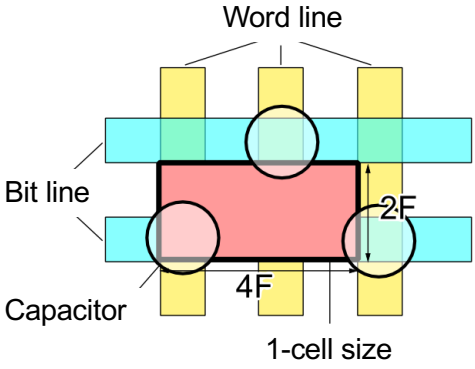


* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/dimension-increase-in-metal-oxide-semiconductor-memories-and-transistors

For Higher Recording Density ...

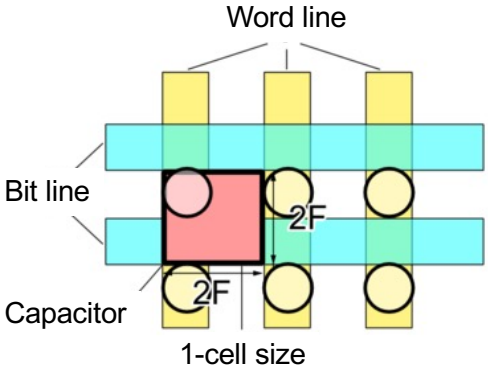
Conventional DRAM cell :

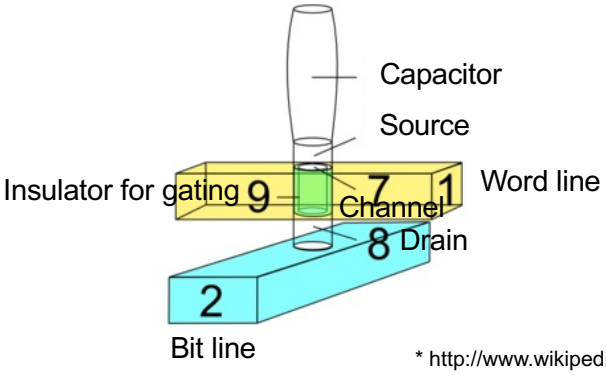
$8F^2$ DRAM Cell



Next-generation DRAM cell :

$4F^2$ DRAM Cell



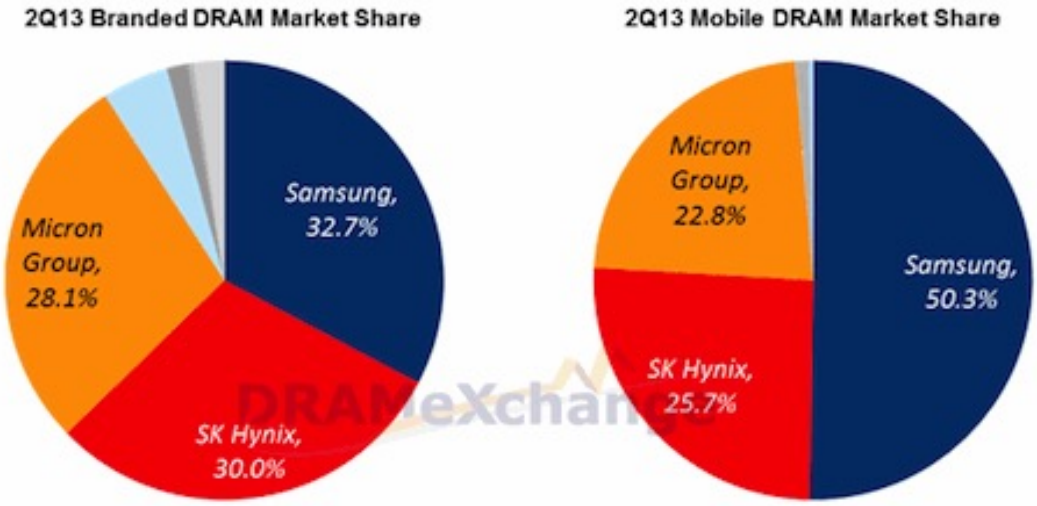


* http://www.wikipedia.org/

DRAM Market

Market dominated by 3 major manufacturers :

Figure-1 2Q13 Brand DRAM & Mobile DRAM Market Share

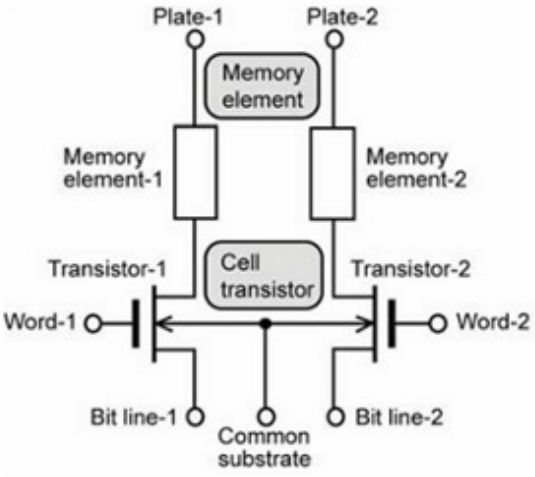


Source: DRAMeXchange, Sept., 2013

* http://www.computerworld.com/s/article/9242145/After_Hynix_plant_fire_spot_market_DRAM_prices_jump_20_

Super Pillar Transistor (SPT)

Universal transistor architecture for various memories :



Memory element	Memory
(a) Capacitor	DRAM
(b) Phase change	PCM
(c) Resister	ReRAM
(d) Magnetic film	MRAM
(e) New material	New memory

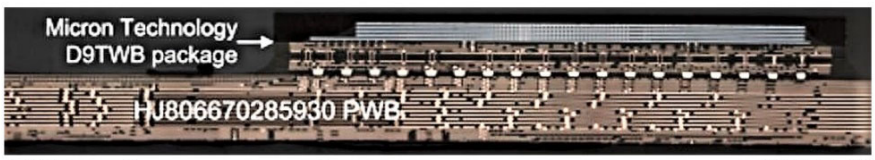
Cell transistor	Memory
(f) Ferroelectric	FeRAM
(g) Floating gate	Flash memory
(h) SiON film	Flash memory
(i) New material	New memory

* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/dimension-increase-in-metal-oxide-semiconductor-memories-and-transistors

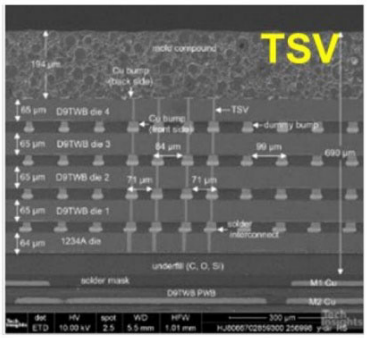
Hybrid Memory Cube

Micron developed hybrid memory cube (HMC) :

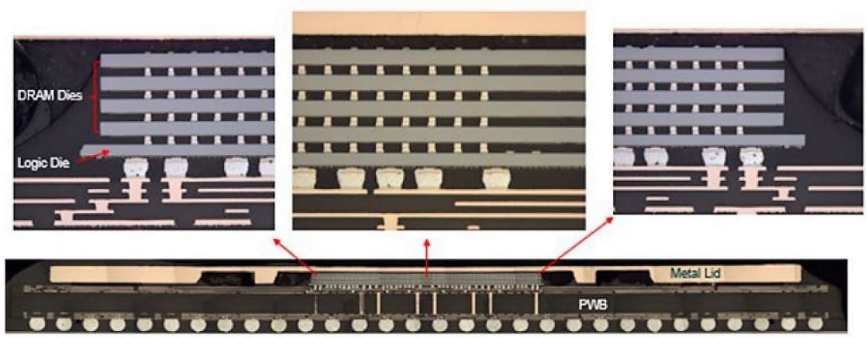
stacks connected by .



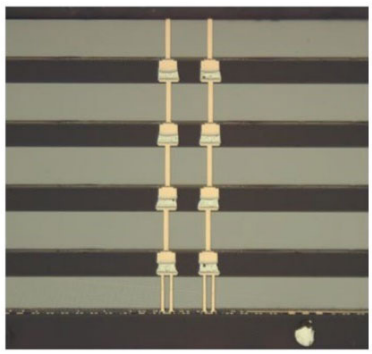
HMC package cross-section



HMC TSVs



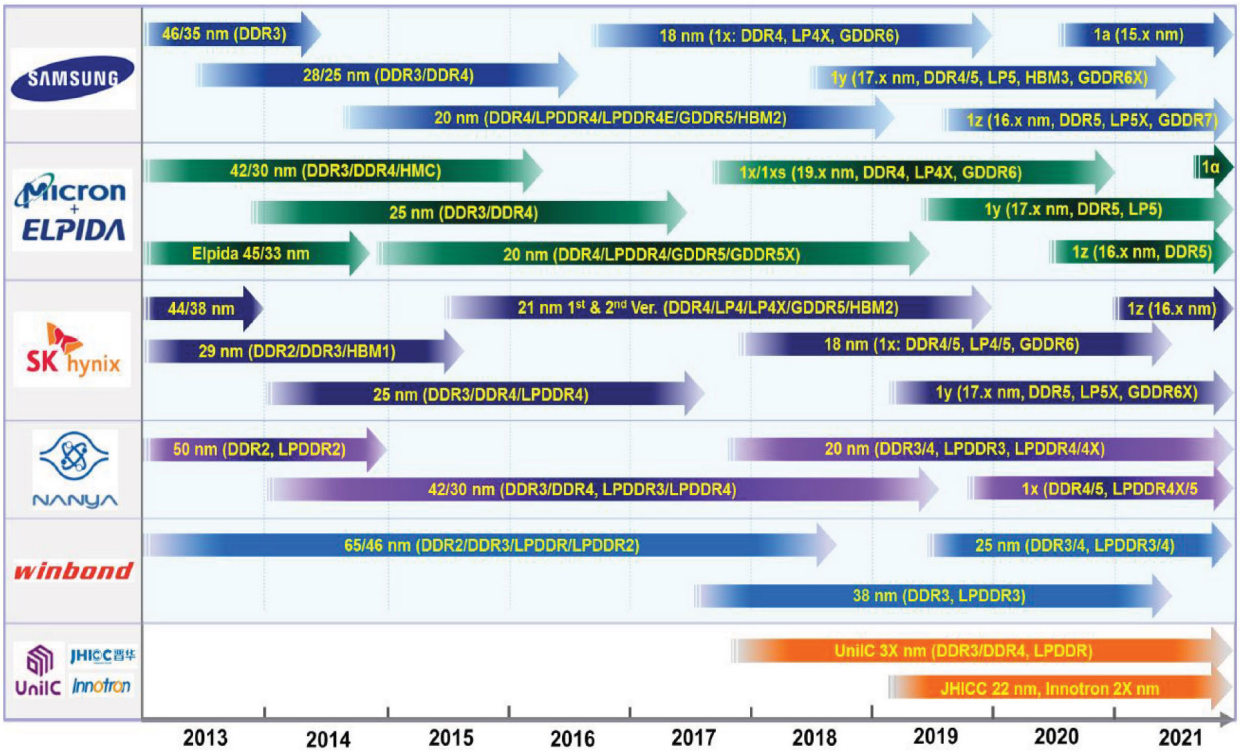
HMC2 package cross-section



HMC2 TSVs

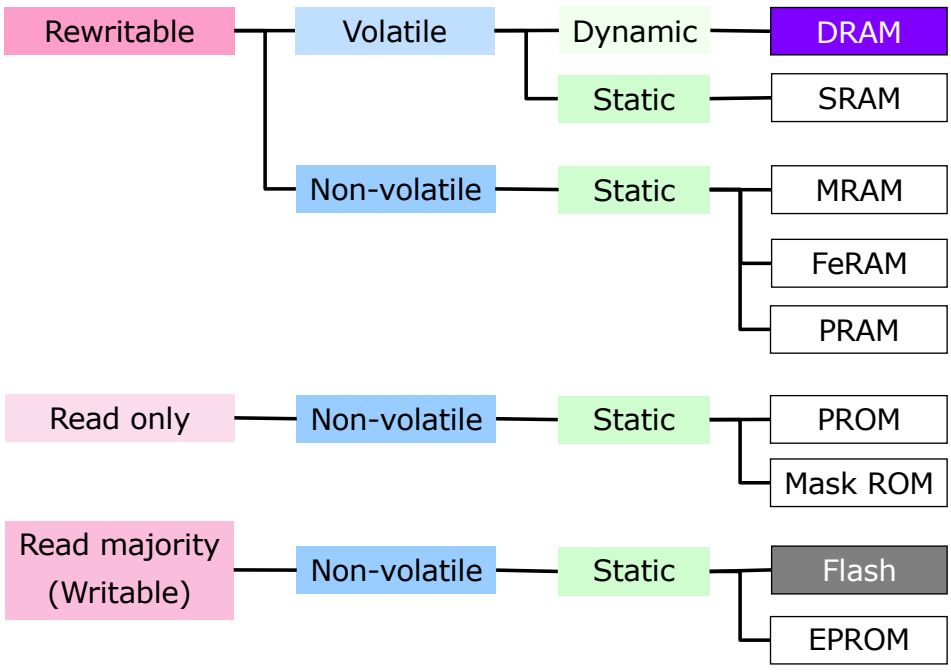
* https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18

DRAM Roadmap



* https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18

Memory Types



* http://www.semiconductorjapan.net/serial/lesson/12.html

Major Memories

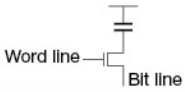
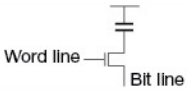
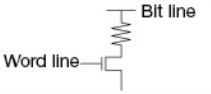
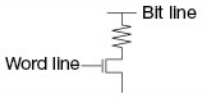
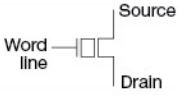
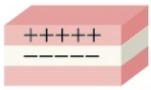
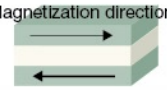
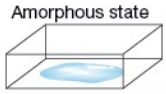
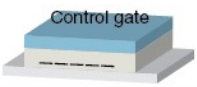
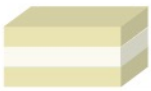
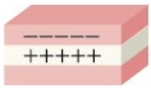
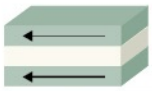
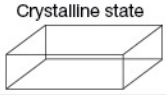
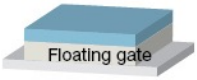
	DRAM	FeRAM	MRAM	PRAM	Flash memory
Storage	Capacitor	Ferroelectric capacitor	TMR device	Phase-change device	Floating gate
Cell equivalent circuit					
"1" storage device					
"0" storage device					
Advantages	• High-speed write/read • Low cost	• Non-volatile • Low current consumption • Medium-speed write/read	• Non-volatile • Effectively infinite number of rewrites • High-speed write/read	• Non-volatile • Easy to manufacture	• Low cost • Non-volatile
Disadvantafes	• High standby current • Volatile	• Scalability (not easy to port to smaller line widths) • Destructive read	• High write current	• High write current • Fewer rewrites than MRAMs, FeRAMs, etc • Rewrite slower than MRAMs, FeRAMs, etc	• Slow write • 10^5 or fewer rewrites

Fig 2 Competition in Dissipation, Speed, Rewrites, Memory Capacity, etc A comparison of the advantages and disadvantages of FeRAMs, MRAMs and PRAMs. DRAMs, Flash memory, etc are also shown for reference. The PRAM cell equivalent circuit shown assumes transistors used for cell selection. The use of diodes for PRAM cell selection is also being developed. NV-RAMs use a data storage method quite different from existing memory. While existing DRAMs, Flash memory, etc determine whether a bit is 0 or 1 from the charge level, NV-RAM store information in the position of atoms in the storage device, magnetic field direction, molecular state, etc. FeRAMs, for example, use a ferroelectric material that generates a monopole when an electric field is applied. MRAMs utilize the change in TMR device magnetization direction caused by an external magnetic field, current, etc. And PRAMs read information by checking if the phase-change material used in the optical disc is crystalline or amorphous.

* http://techon.nikkeibp.co.jp/article/HONSHI/20070926/139715/