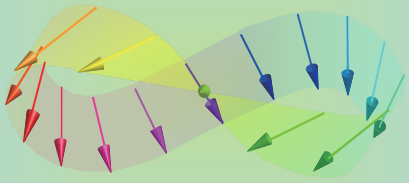
Information Storage and Spintronics 10



Atsufumi Hirohata

Department of Electronic Engineering

THE UNIVERSITY of York

14:00 Friday, 28/October/2022 (SLB 101)

Quick Review over the Last Lecture

DRAM :

Data stored in a capacitor.

→ Electric charge needs

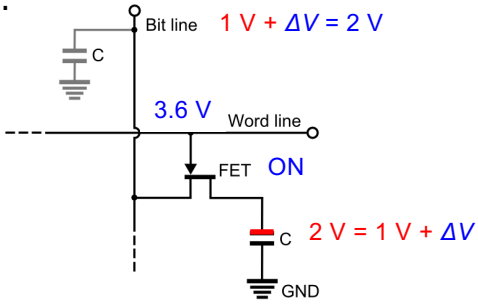
→ DRAM requires

Read-out operation of 1C1T :

" "-data :

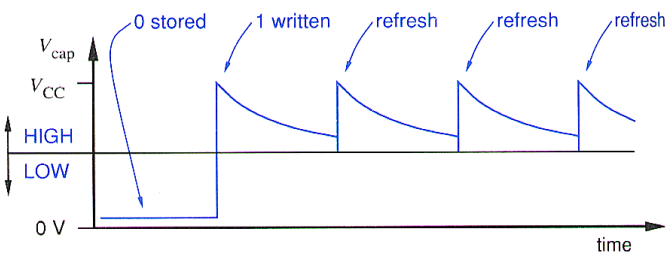
.

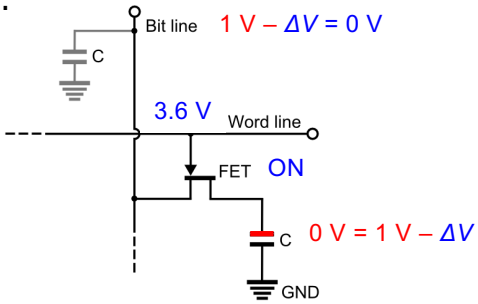
.



Refresh operation of :

" "-data :



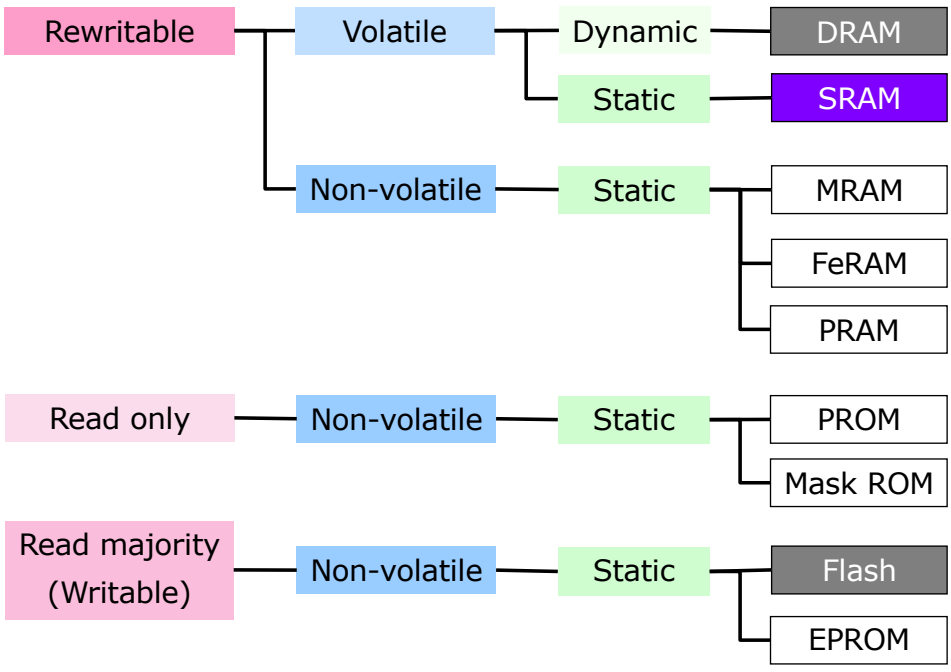


* http://www.wikipedia.org/;
* http://users.cis.fiu.edu/~prabakar/cda4101/Common/notes/lecture09.html

10 Static Random Access Memory

- Volatile memory developmement
- 6T-SRAM architecture
- Read / write operation
- 1T-SRAM
- Various ROMs

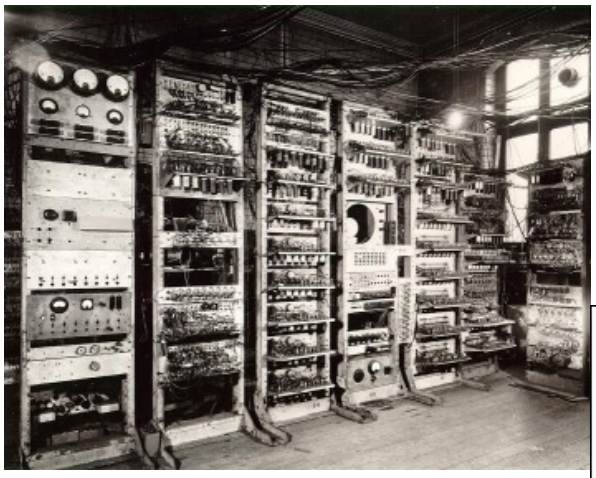
Memory Types

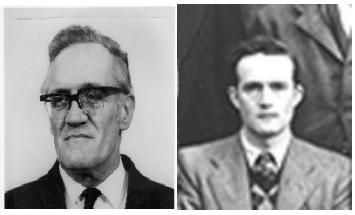


* http://www.semiconductorjapan.net/serial/lesson/12.html

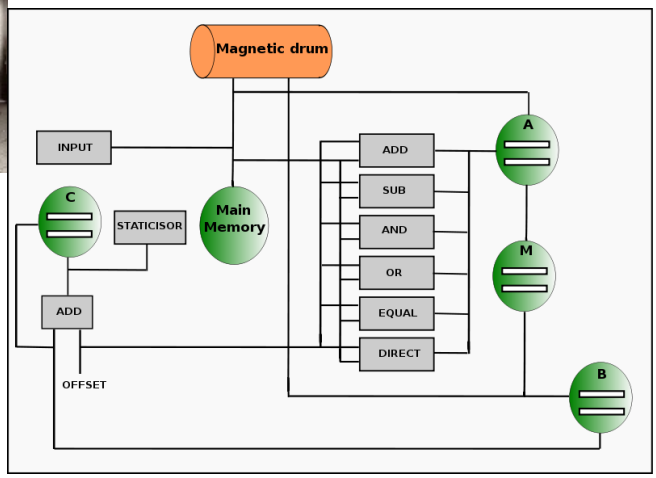
Manchester Automatic Digital Machine

In 1949, Frederic C. Williams and Tom Kilburn developed Manchester Mark 1 :





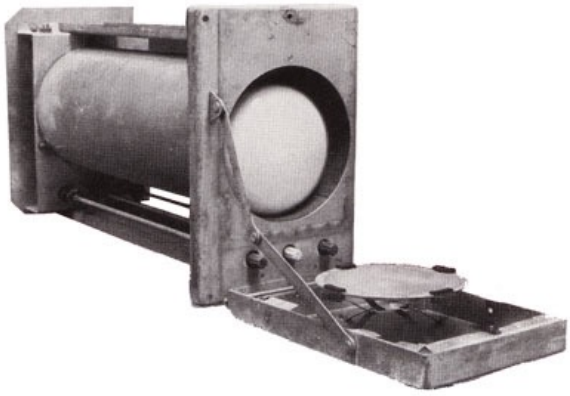
One of the earliest computers



* http://www.computer50.org/mark1/;
** http://www.wikipedia.org/

Williams-Kilburn Tube

Cathode-ray tube to store data :



Utilise a of electron charges at a fluorescent screen when an electron hit it.

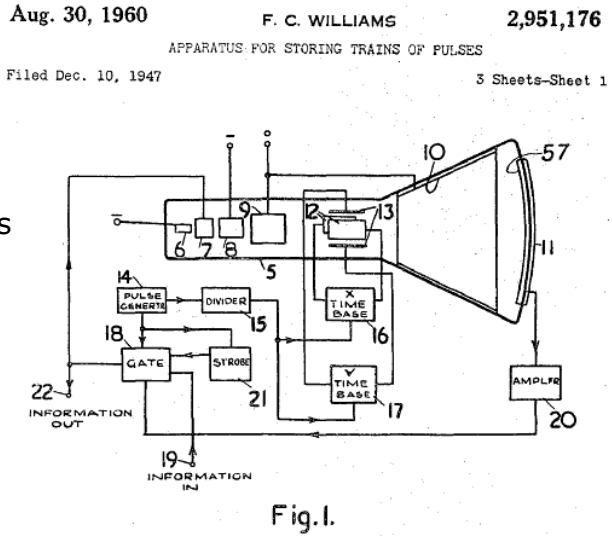
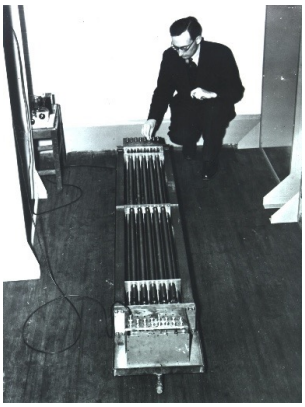

Aug. 30, 1960 F. C. WILLIAMS 2,951,176
APPARATUS FOR STORING TRAINS OF PULSES
Filed Dec. 10, 1947 3 Sheets-Sheet 1

Fig. 1.

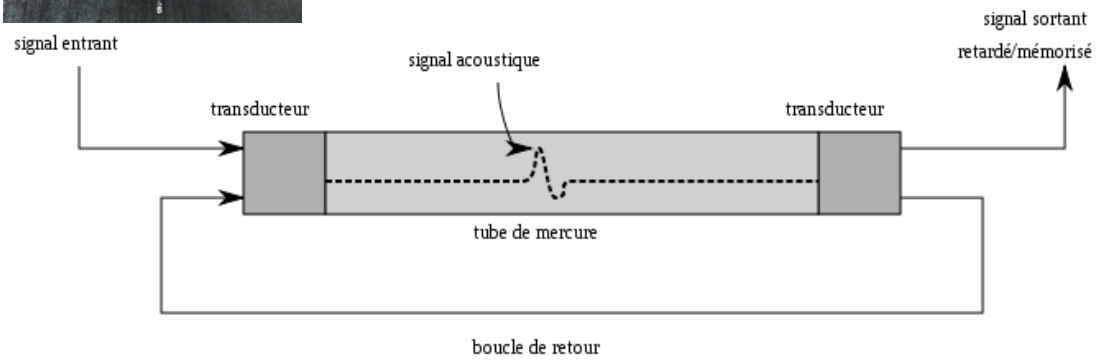
* http://www.wikipedia.org/

Delay Line Memory

In 1947, John P. Eckart invented a mercury delay line memory :



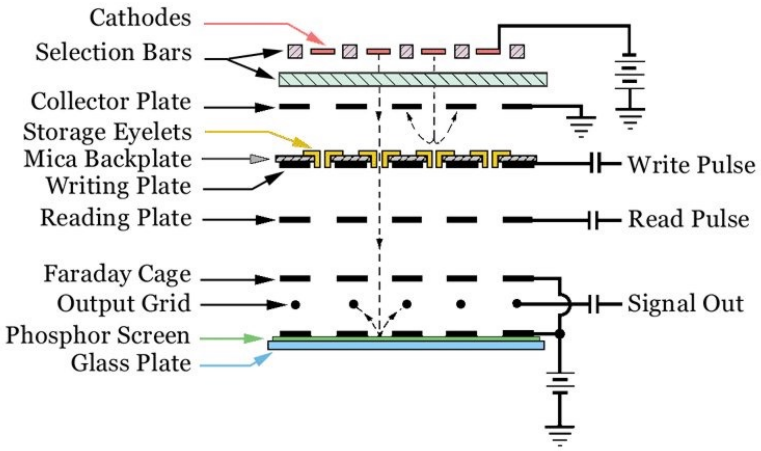
Utilise an
generated by a transducer
to store a data.



* http://www.wikipedia.org/

Selectron Tube

In 1953, Jan A. Rajchman (RCA) invented a selectron tube :

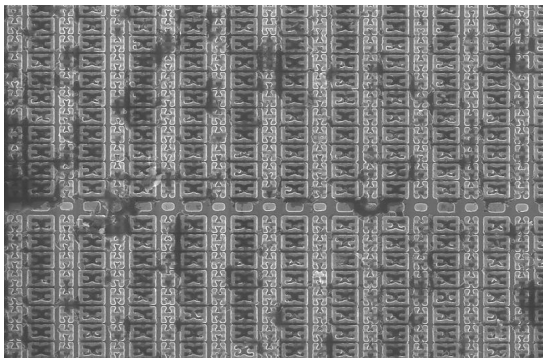


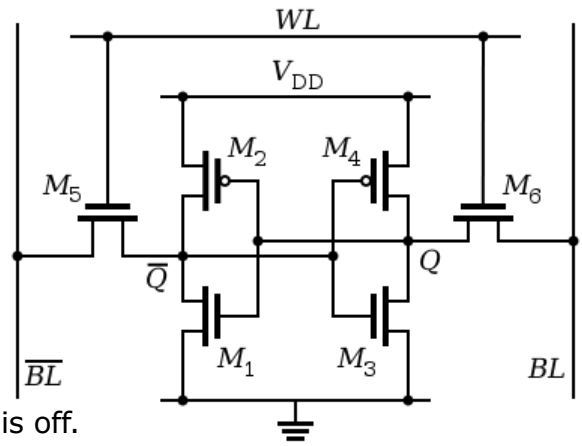
An array of is used to store data electrostatically.

* http://www.ieeeghn.org/wiki/index.php/Jan_Rajchman;
** http://www.wikipedia.org/

Static Random Access Memory (SRAM)

Static random access memory (SRAM) :



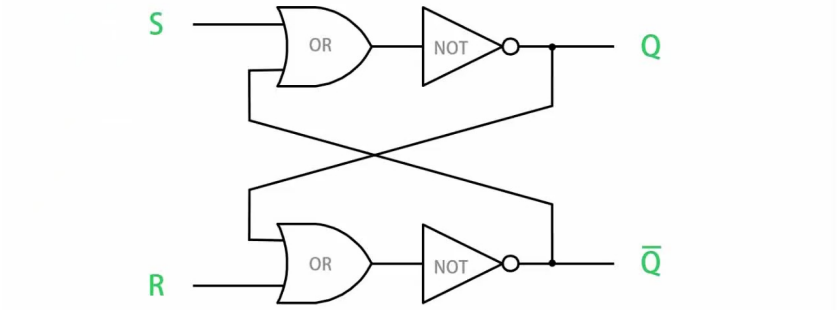


No need to data.

→ Even so, the data is lost once the power is off.

Flip flop is used to store data.

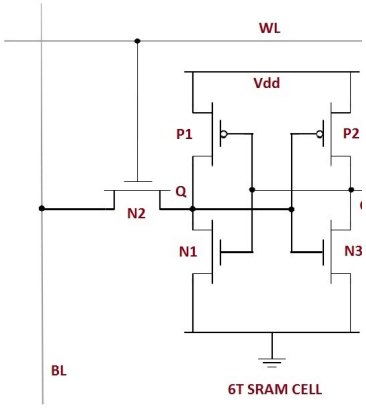
→

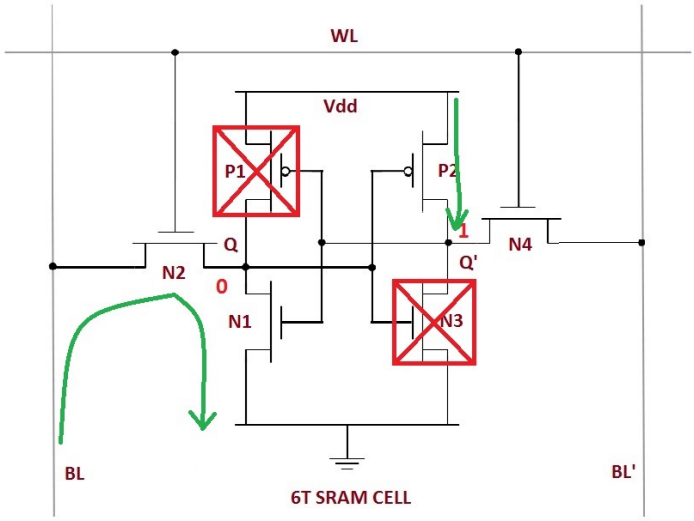


* http://www.wikipedia.org/; https://www.youtube.com/watch?v=4vAGaWyGanU

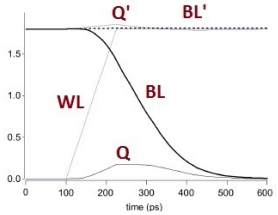
6T-SRAM Read Operation

A standard SRAM cell :





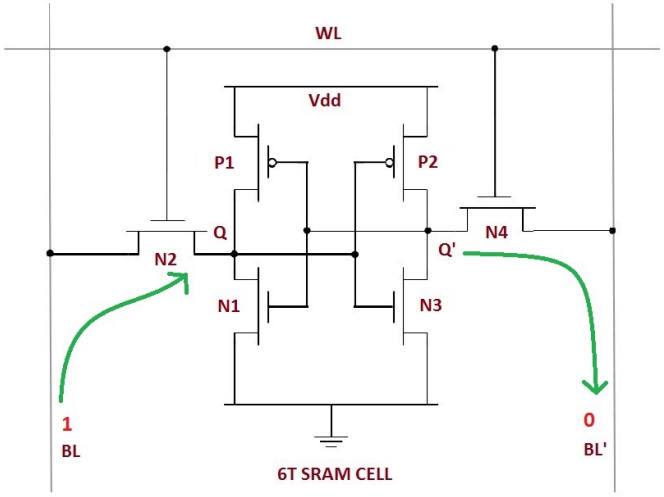
READ OPERATION: i) Precharge BL, BL' to HIGH
ii) Turn on WL
iii) BL or BL' will be pulled down to LOW depending on Q, Q'
iv) Eg. If Q = 0, Q'= 1, BL discharges through N2 - N1 - GND and BL' stays high. But Q bumps up slightly
v) In order for Q to not flip N1 should be stronger than N2, i.e N1 >> N2

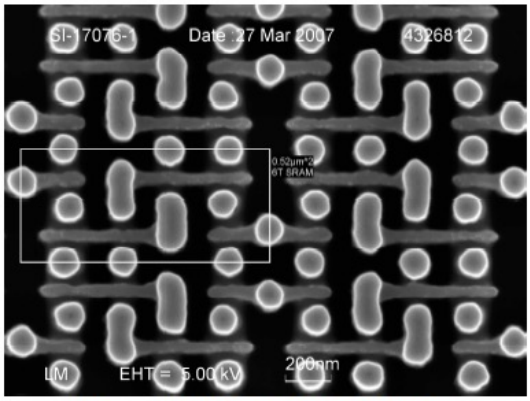


* http://allthingsvlsi.wordpress.com/tag/6t-sram-operation/

6T-SRAM Write Operation

Write operation :

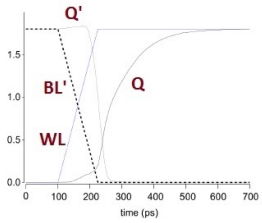




65nm TSMC 6T SRAM

WRITE OPERATION: i) Drive BL, BL' with necessary values
ii) Turn on WL
iii) Bit Lines overpower cell with new value
iv) Eg. Q = 0, Q' = 1 and BL = 1, BL' = 0. This forces Q' to low and Q to high
v) To overpower feedback inverter loop, N2 should be stronger than P1, i.e N2 >> P1

As Q starts to charge up to 1, output of inverter P2-N3 starts to discharge which in turn, makes P1 turn on. Thus the feedback inverters lock on to the values to be written



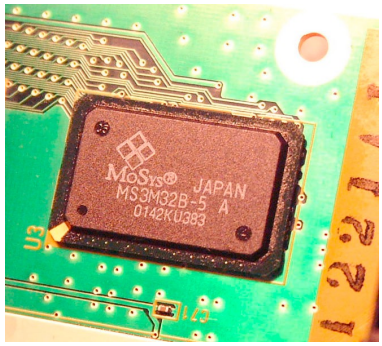
* http://allthingsvlsi.wordpress.com/tag/6t-sram-operation/
** https://cseweb.ucsd.edu/classes/fa11/cse240A-a/Slides1/02_Technology-2.pdf

6T-SRAM Operation

* https://www.youtube.com/watch?v=kU2SsUUsftA

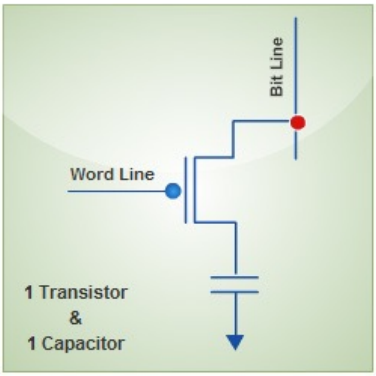
1T-SRAM

Pseudo SRAM developed by MoSys :



By comparing with the conventional 6T-SRAM,

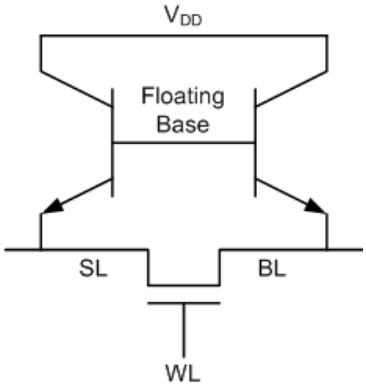
- ✓ < 1/3 area
- ✓ power consumption
- ✓ to be embeded
- ✓ interface
- ✓ Similar to SRAM performance
- ✓ latency as compared with DRAM
- ✓ fidelity (< 1 FIT / Mbit, FIT : failure in time of 10^9 hours)

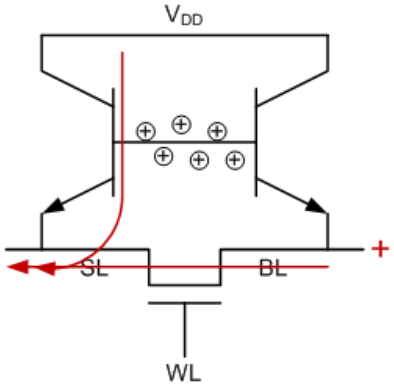


* http://www.wikipedia.org/;
** http://www.mosys.com/high-density-memory.php

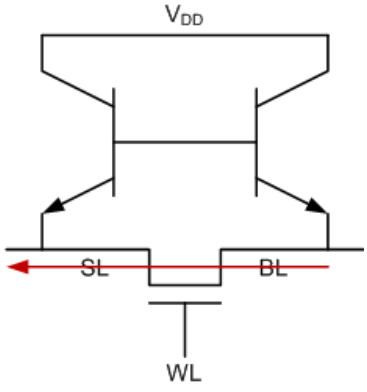
1T-SRAM Operation

Transistor used similar to DRAM :





Programmed

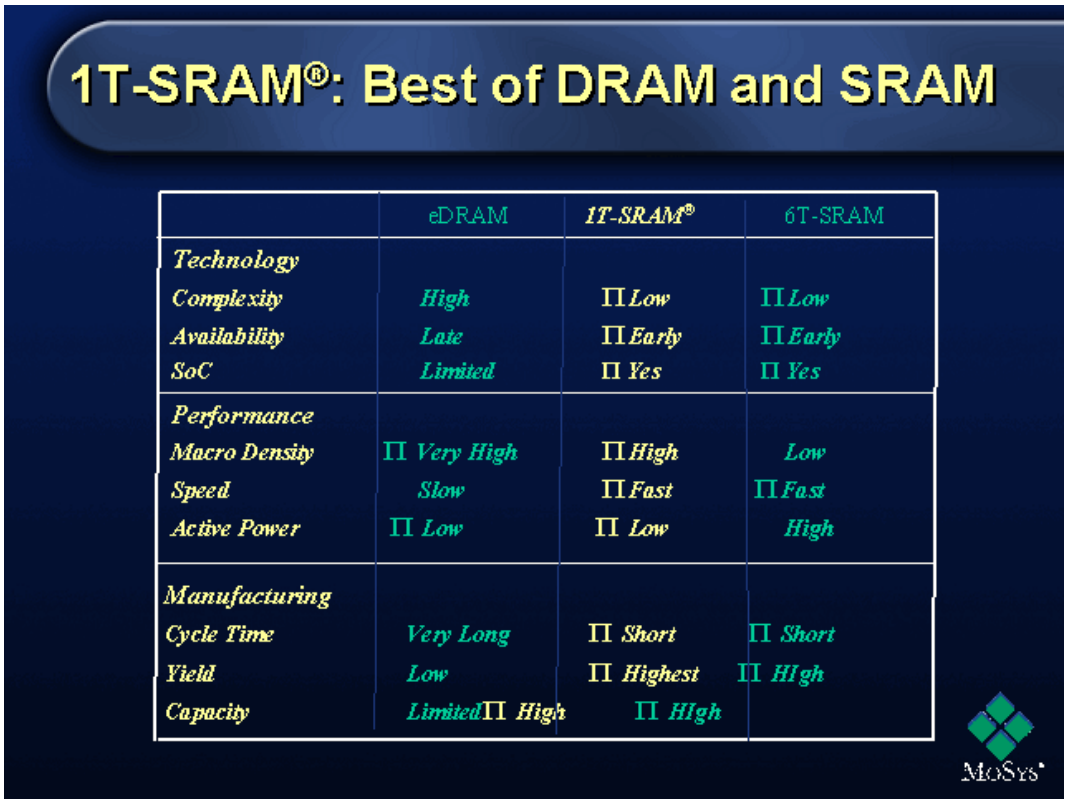


Erased

* https://www.eejournal.com/article/20160104-zeno/

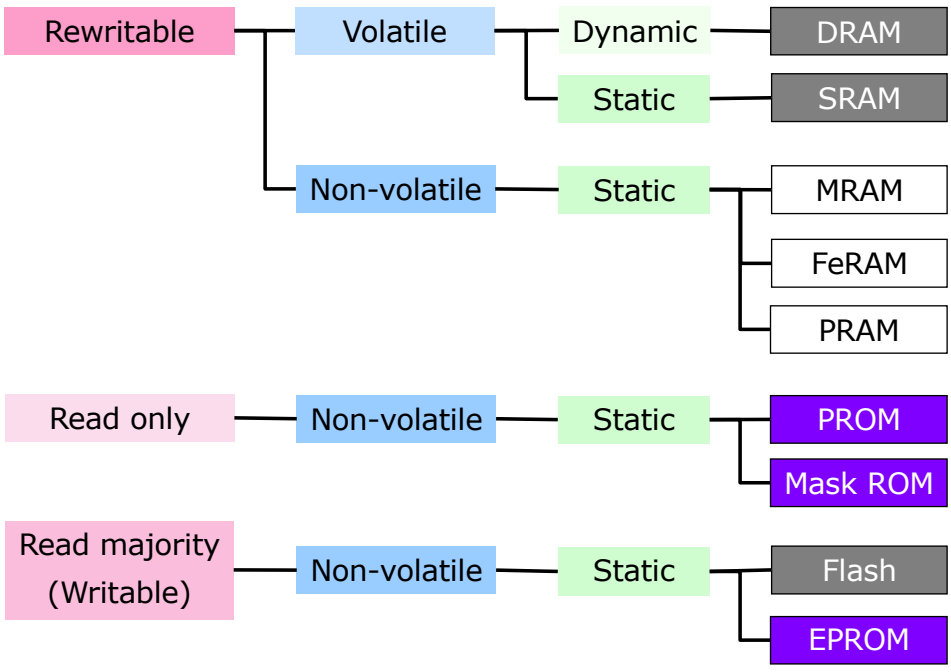
Advantages of 1T-SRAM

Comparison between 1T-SRAM, embedded DRAM (eDRAM) and 6T-SRAM :



* http://media.corporate-ir.net/media_files/nsd/mosy/presentations/corp_pres_1103/sld012.htm

Memory Types

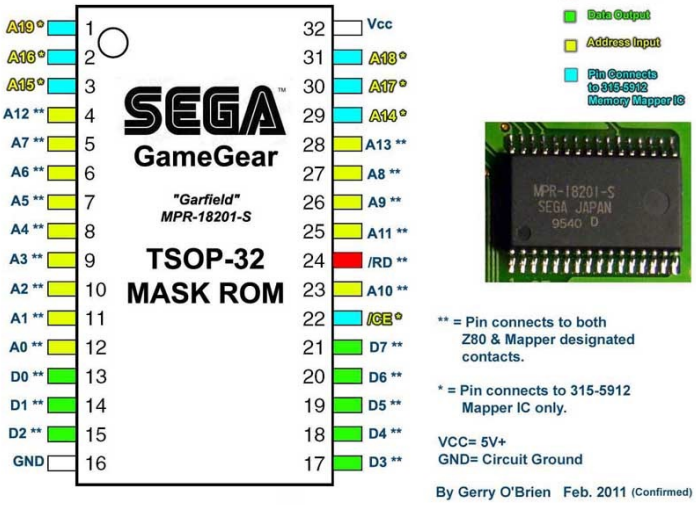


* http://www.semiconductorjapan.net/serial/lesson/12.html

Mask ROM

Read-only memory made by a photo-mask :

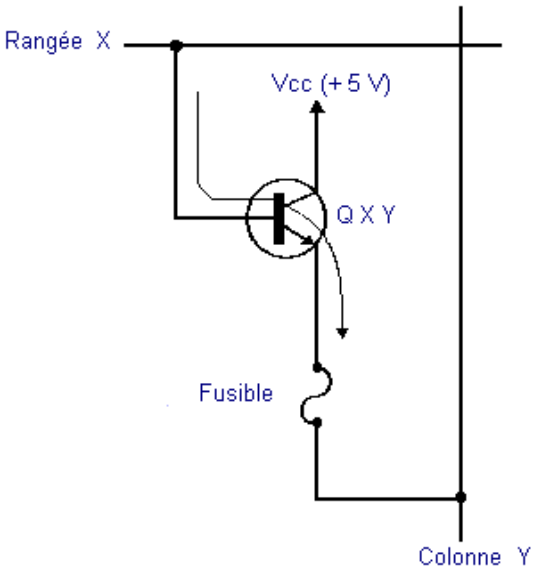
- ✓ Cheap
- ✓ Simple structure
- ✓ Ideal for integration
- × Initial mask fabrication cost
- × Lead time for mask fabrication
- × No design change without mask replacement



* http://www.smspower.org/Development/MaskROMs

Programmable ROM (PROM)

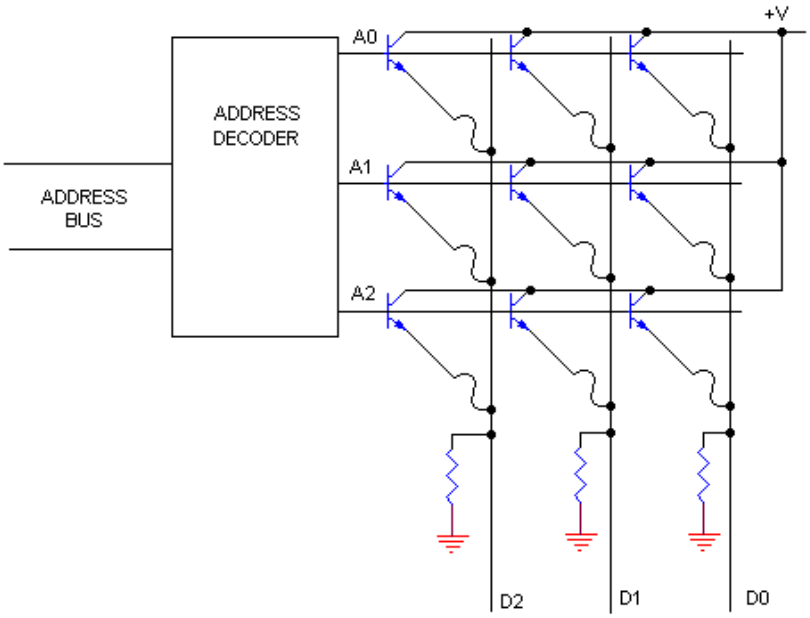
PROM bipolar cell :



* http://www.electronics.dit.ie/staff/tscarff/memory/rom.htm

PROM Architecture

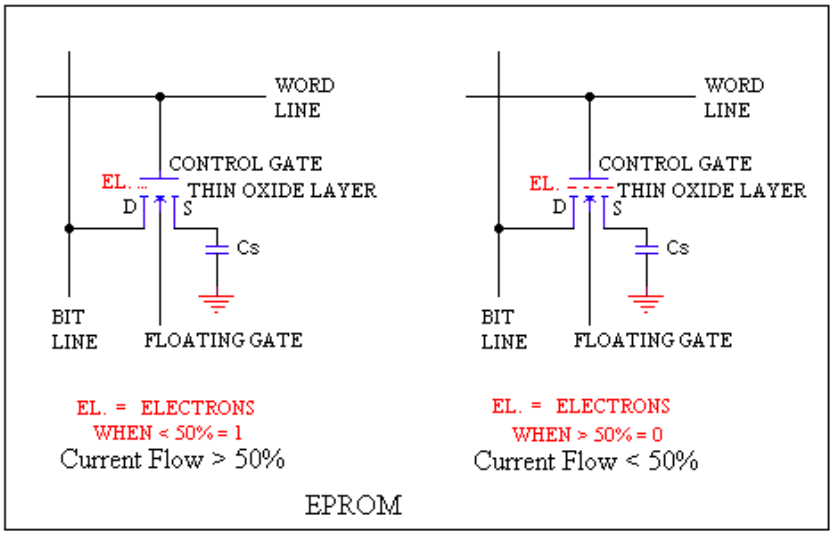
PROM architecture :

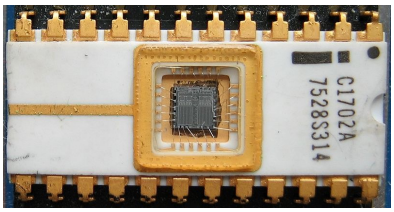


* http://www.electronics.dit.ie/staff/tscarff/memory/rom.htm

Erasable PROM

UV-light can erase stored data :





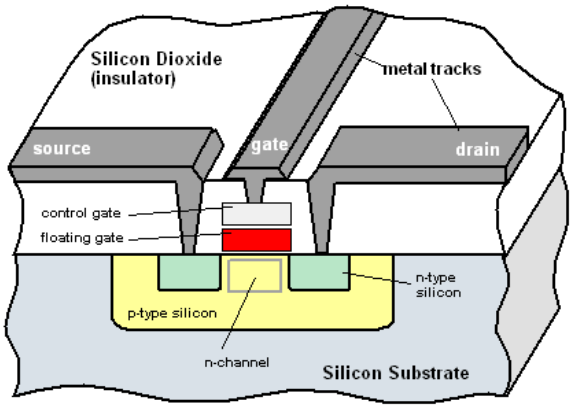
* http://www.wikipedia.org/;
* http://www.electronics.dit.ie/staff/tscarff/memory/rom.htm

Electrically EPROM (EEPROM)

In 1978, George Perlegos (Intel) developed electrical erasing mechanism :

- ✓ to flash memory
- ✓ Individual bits are erasable.
- ✓ Rewritable by simply writing a new data
- ✓ Rewritability times
- × capacity (~ bytes)
- × More complicated architecture as compared with flash memory
- × Higher cost for fabrication as compared with flash memory

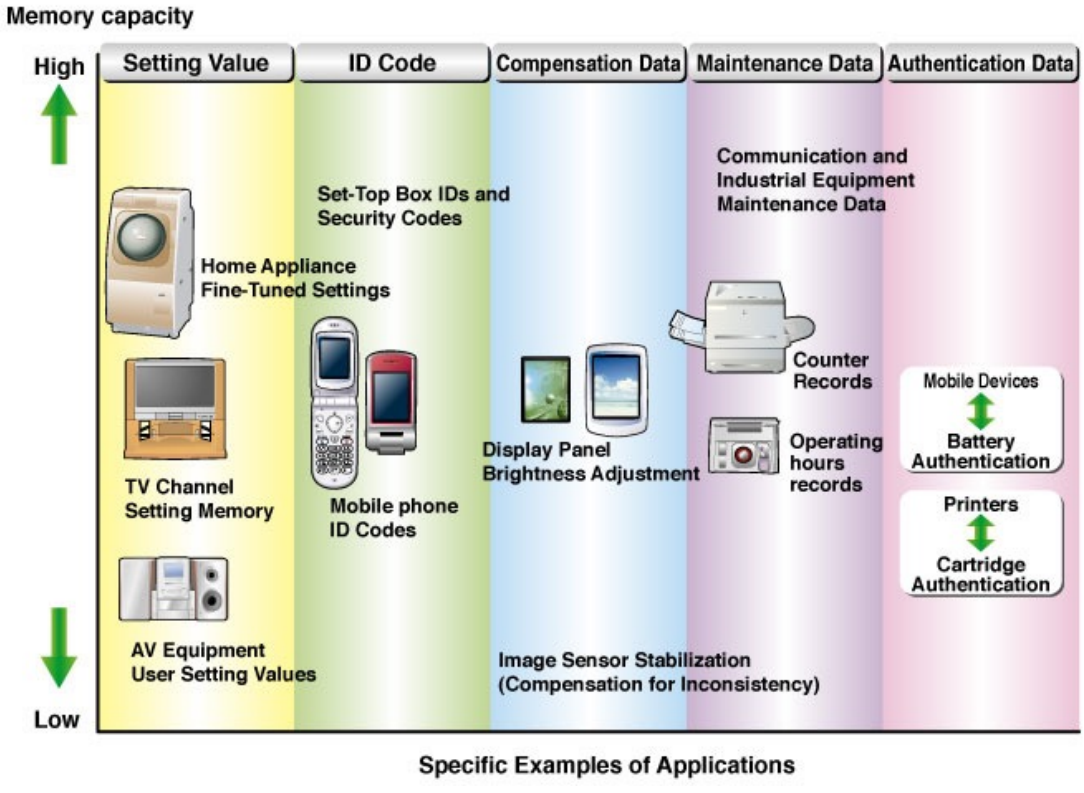
EEPROM and Flash Transistor



* http://www.answers.com/topic/eeprom

EEPROM Usages

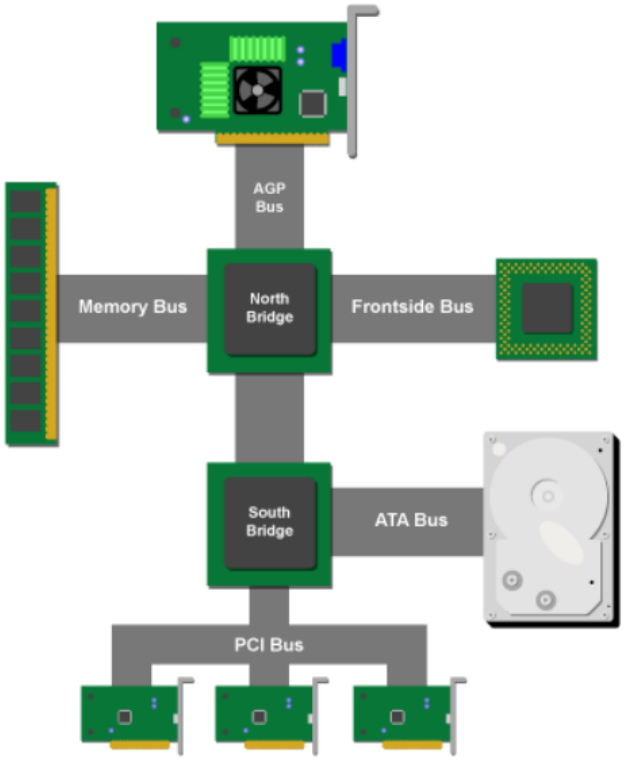
EEPROM is used in various applications :



* http://www.sanyosemi.com/en/memory/topics/serial-eeprom.php

Connections between the Components

Connections between CPU, in/outputs and storages :



* http://testbench.in/introduction_to_pci_express.html;