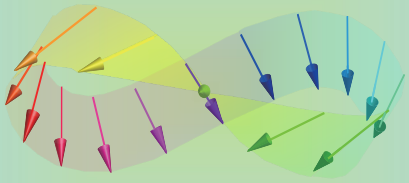
Information Storage and Spintronics 11



Atsufumi Hirohata

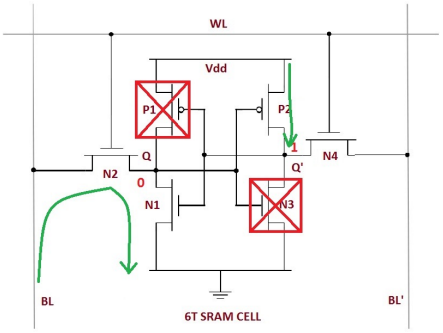
Department of Electronic Engineering

THE UNIVERSITY of York

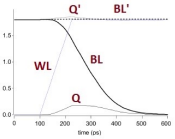
14:00 Monday, 07/November/2022 (SLB 101)

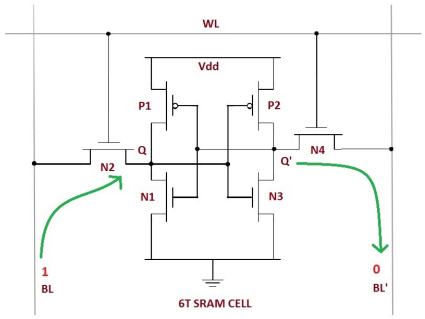
Quick Review over the Last Lecture

6T-SRAM (static random access memory) operation :



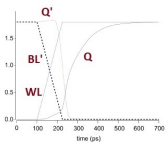
READ OPERATION: i) Precharge BL, BL' to HIGH
ii) Turn on WL
iii) BL or BL' will be pulled down to LOW depending on Q, Q'
iv) Eg. If Q = 0, Q' = 1, BL discharges through N2 - N1 - GND and BL' stays high. But Q bumps up slightly
v) In order for Q to not flip N1 should be stronger than N2, i.e N1 >> N2



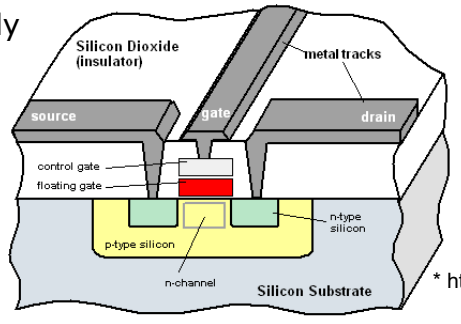


WRITE OPERATION: i) Drive BL, BL' with necessary values
ii) Turn on WL
iii) Bit Lines overpower cell with new value
iv) Eg. Q = 0, Q' = 1 and BL = 1, BL' = 0. This forces Q' to low and Q to high
v) To overpower feedback inverter loop, N2 should be stronger than P1, i.e N2 >> P1

As Q starts to charge up to 1, output of inverter P2-N3 starts to discharge which in turn, makes P1 turn on. Thus the feedback inverters lock on to the values to be written



EEPROM (electrically erasable read only memory) :

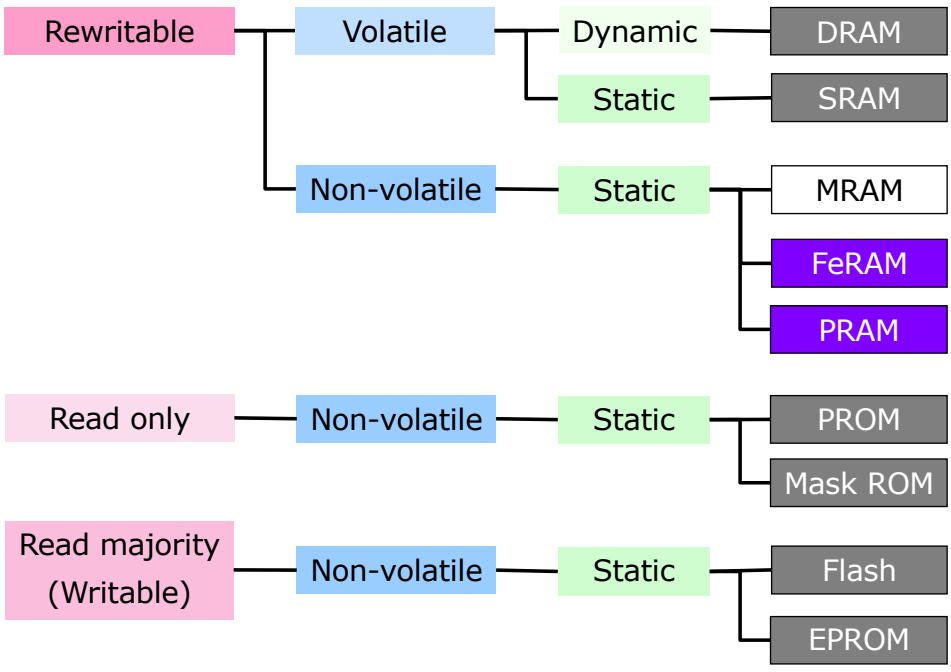


* http://allthingsvlsi.wordpress.com/tag/6t-sram-operation/;
* http://www.answers.com/topic/eeprom

11 Ferroelectric / Phase Change Random Access Memories

- FeRAM
- PRAM
- ReRAM

Memory Types



* http://www.semiconductorjapan.net/serial/lesson/12.html

Comparison between Next-Generation Memories

Table 1 Representative NV-RAM Available 2007-08 Comparison of large-capacity NV-RAM chips available on the merchandise market.

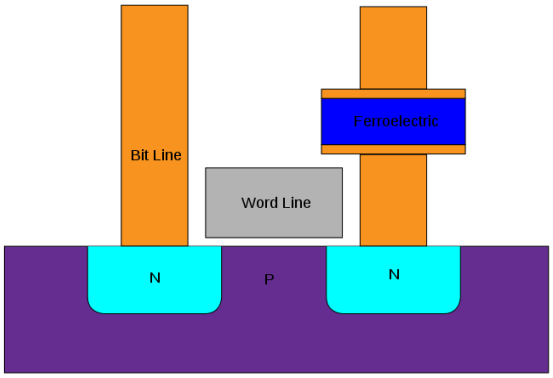
Memory type		FeRAM (ferroelectric memory)		MRAM (magnetic memory)	PRAM (phase-change memory)	
Manufacturer		Fujitsu	Ramtron International	Freescale Semiconductor	Intel	Samsung Electronics
Model		MB85R2001/ MB85R2002	FM22L16	MR2A16A	Not disclosed	Not disclosed
Capacity		2-Mbit	4-Mbit	4-Mbit	128-Mbit/1-Gbit/2-Gbit	512-Mbit*1
Word configuration		256Kwords x 8/128Kwords x 16	256Kwords x 16	256Kwords x 16	Not disclosed	32Mword x 16*1
Access time		100ns	55ns	35ns	Read equivalent to DRAM, NOR Flash memory, etc	Not disclosed
Cycle time		150ns	110ns	35ns	Read time tens of ns to 100ns, equivalent to DRAM, NOR Flash memory, etc. Write expected to be significantly faster than NOR Flash memory, but slightly longer than DRAM.*2	Write about 1/30th of NOR Flash memory*2
Operating current consumption	Read	15mA	18mA	80mA	Not disclosed	Not disclosed
	Write	15mA	18mA	155mA	Not disclosed	Not disclosed
Standby current		50μA	150μA	12mA	Not disclosed	Not disclosed
Rewrites		10^{10} or higher	10^{14} times or higher	Effectively infinite (more than 10^{15} times)	10^{9} times or higher	10^{5} times or higher*1
Supply voltage		3V to 3.6V	2.7V to 3.6V	3V to 3.6V	3V /3V /1.8V	1.8V*1
Operating temperature		-20°C to +85°C	-40°C to +85°C	0 to +70°C (general use), -40°C to +85°C (industrial use), -40°C to +105°C (expanded temp range)	Not disclosed	Not disclosed
Data retention time		10 years min (+55°C)	10 years	20 years	10 years min (+85°C)	10 years min (+85°C)*1
Interface		Pseudo-SRAM compliant with asynchronous SRAM	Asynchronous SRAM	Asynchronous SRAM	Not disclosed	Not disclosed
Package		48-pin TSOP	44-pin TSOP	44-pin TSOP	Not disclosed	Not disclosed
Manufacturing technology		180nm	130nm	Not disclosed	90nm/45nm/45nm	90nm*1
Memory cell configuration		1 transistor + 1 capacitor	1 transistor + 1 capacitor (stacked)	1 transistor + 1 TMR device	Not disclosed	1 diode + 1 phase-change device
Memory cell area		Not disclosed	0.71μm²	Not disclosed	Not disclosed	0.0467μm²
Sample shipment start		Samples shipping	Samples shipping	Samples shipping	3Q 2007 / Not disclosed / Not disclosed	2008
Volume production start		Volume production stance established	Small-lot production from 3Q 2007, volume production from 4Q 2007	General-application chips in volume production now	Early 2008 /2H or later 2008 /2H 2008	Not disclosed
Chip manufacturing		In-house	Outsourced to Texas Instruments	In-house	In-house	In-house
Price		Samples ¥2000	US$19.00 in lots of 10,000	US$14.99 in lots of 10,000 for general use, US$24.99 in lots of 10,000 for expanded temp range	Not disclosed	Not disclosed

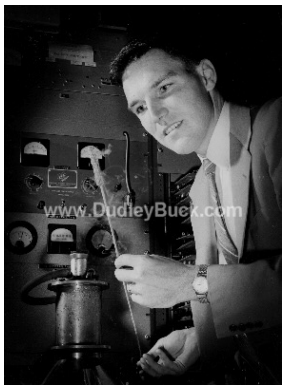
*1 Specifications for Samsung Electronics products have not been disclosed. Specifications shown are those announced at IEDM 2006 by Samsung Electronics in December 2006 for a 512-Mbit prototype.
*2 Most NOR Flash memory has a write time (per-byte) of about 6μs to 7μs.

* http://techon.nikkeibp.co.jp/article/HONSHI/20070926/139715/

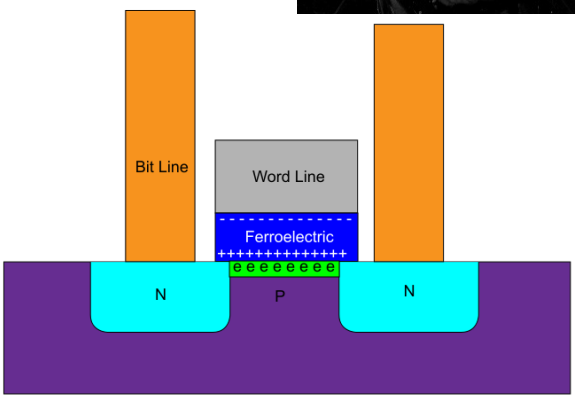
Ferroelectric Random Access Memory (FeRAM)

In 1952, Dudley A. Buck invented ferroelectric RAM in his master's thesis :





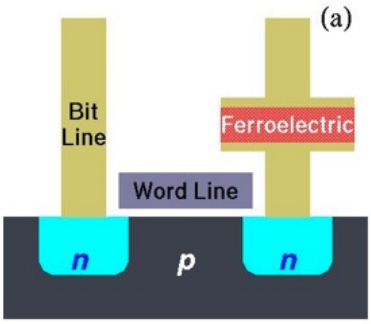
- ✓ Utilise ferroelectric polarisations
- ✓ Very fast latency : < ns
- ✓ CMOS process compatible
- × Relatively large cell size : F^2
- × Destructive read-out

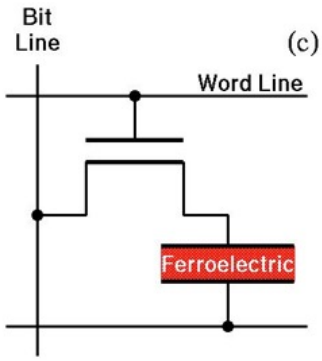


* http://www.DudleyBuck.com/;
** http://www.wikipedia.org/

FeRAM Cells 1

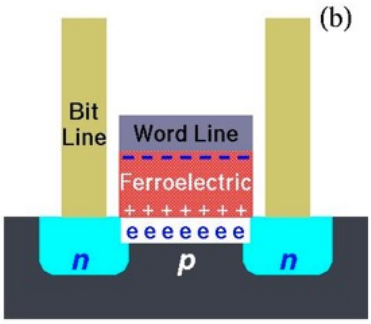
1-transistor 1-capacitor type :

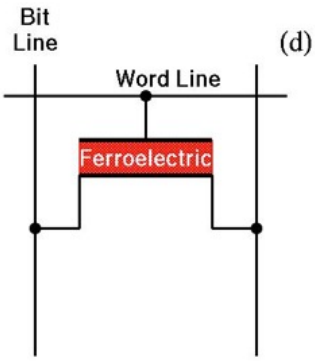




1T1C type

1-transistor type :



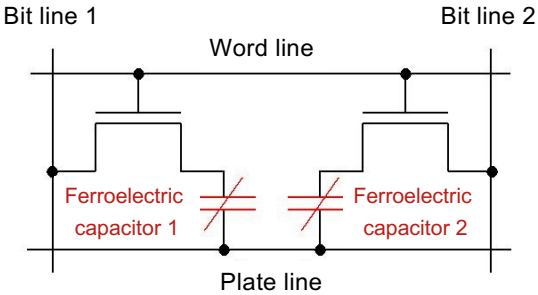


1T type

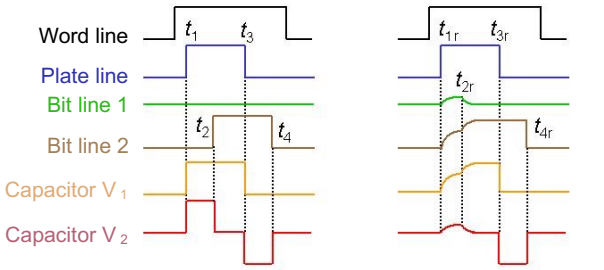
* http://loto.sourceforge.net/feram/doc/film.xhtml

FeRAM Cells 2

2-transistor 2-capacitor type :



2T2C型



FeRAM Writing operation Reading operation

✓Prevent destructive read-out

* http://www,wikipedia.org/

FeRAM Operation

* https://www.youtube.com/watch?v=vppR8EIb_6I

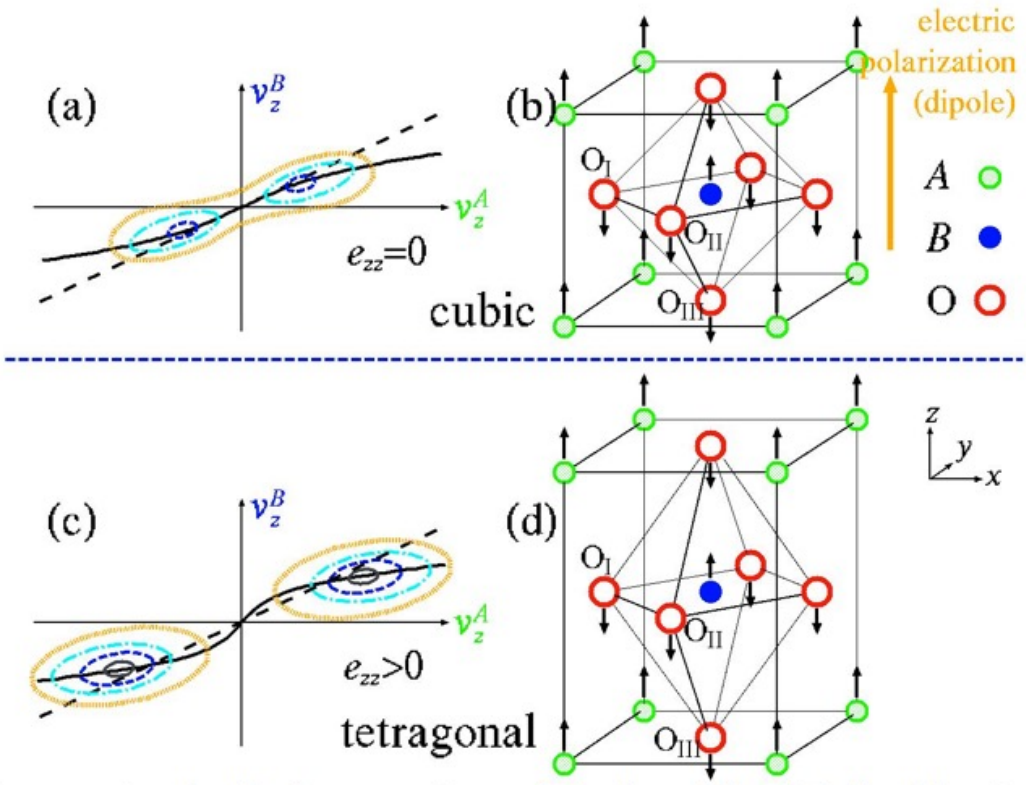
Requirements for Ferroelectric Materials

FeRAM cell structure :

- Large residual polarisation
  → recording density
- Small dielectric constant
  → Read-out error reduction
- Small coercive electric field
  → power consumption
- High fatigue endurance
  → -year usage (> 10^{12} polarisation reversal)
- High remanence
  → -year tolerance for data
- Small imprint
  → recording density

Ferroelectric Materials

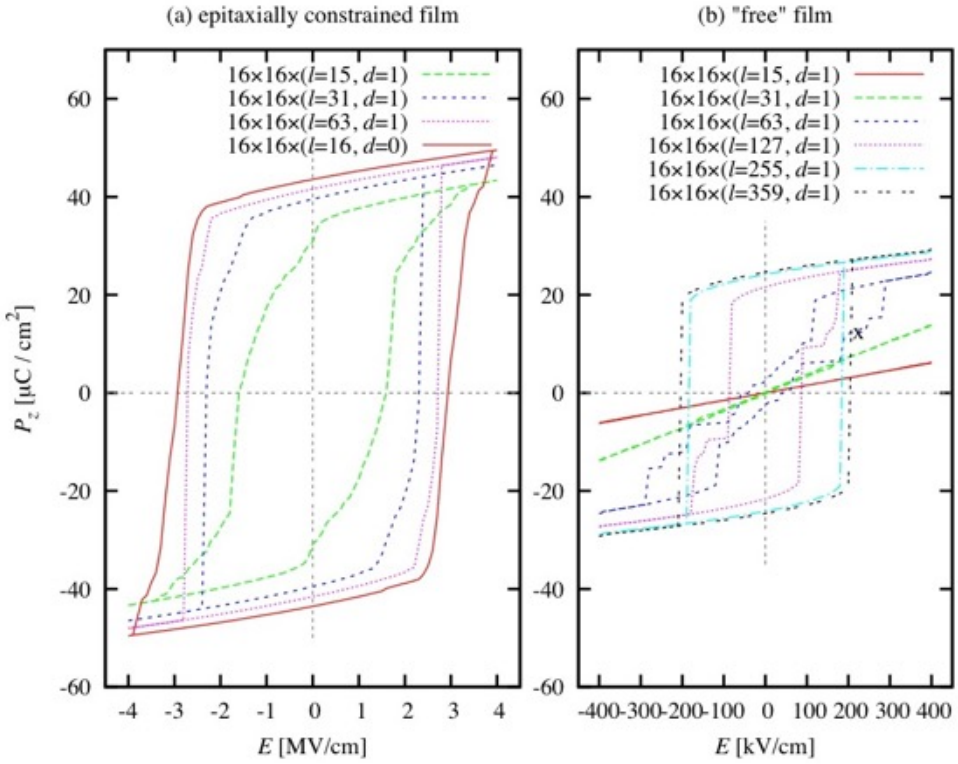
ABO_3 type materials :



* http://loto.sourceforge.net/feram/doc/film.xhtml

Polarisation Hysteresis

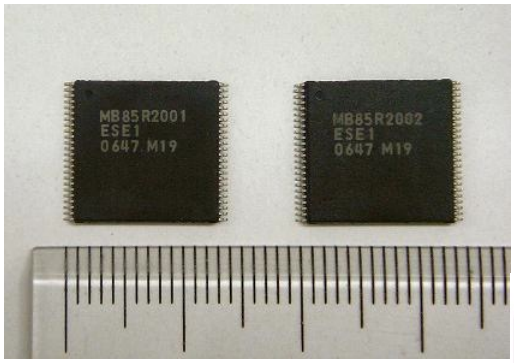
For example, $BaTiO_3$:

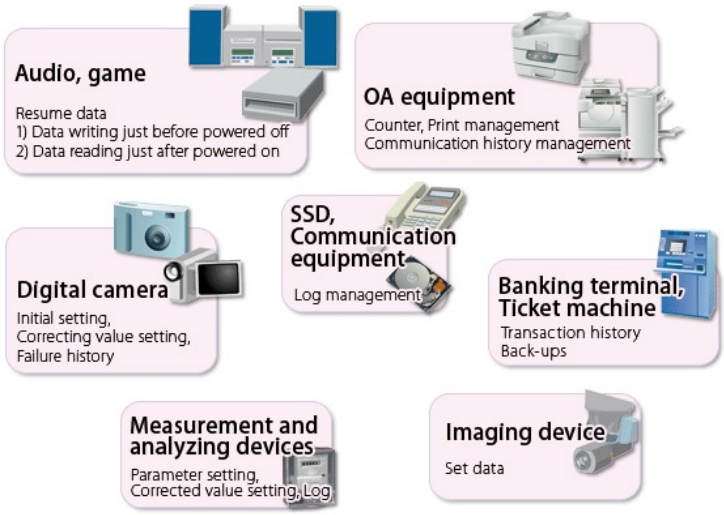


* http://loto.sourceforge.net/feram/doc/film.xhtml

Applications

2-Mb FeRAM introduced by Fujitsu :





* http://www.fujitsu.com/

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*2 Most NOR Flash memory has a write time (per-byte) of about 6μs to 7μs.

* http://techon.nikkeibp.co.jp/article/HONSHI/20070926/139715/

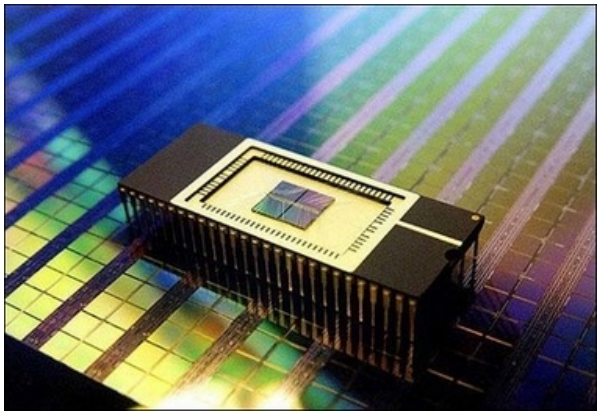
Phase Change

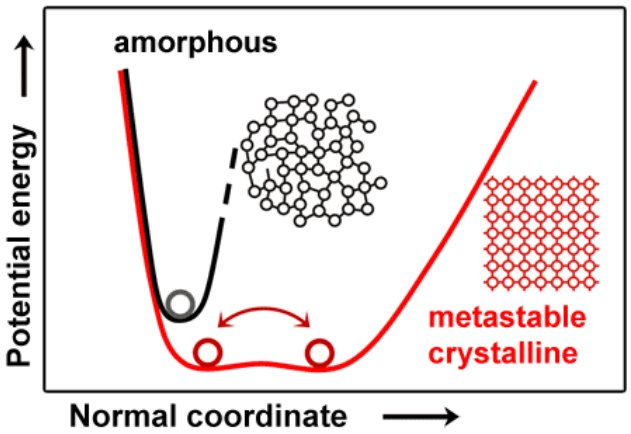
In 1960s, Stanford R. Ovshinsky studied phase-change properties of chalcogenide

In 1969, Charles Sie demonstrated the feasibility for memory applications.

In 1999, Ovonyx was established for memory realisation :

- 512 Mbit (Samsung, 2006)
- 1 Gbit (Numonyx, 2009)
- 1.8 Gbit (Samsung, 2011)

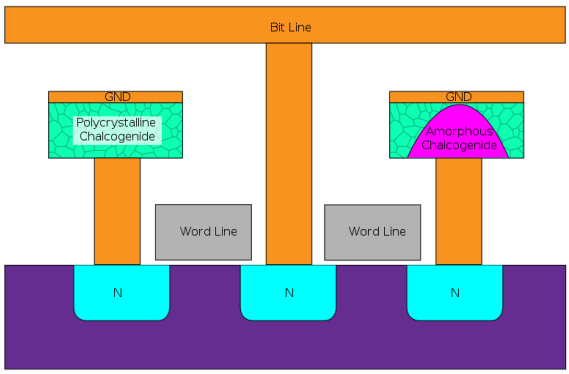


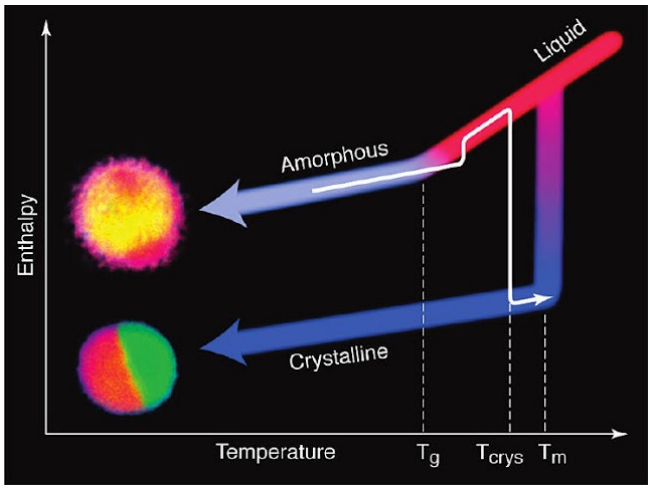


* http://www.esrf.eu/news/general/phase-change-materials/index_html;
** http://www.careace.net/2010/05/06/samsung-introducing-phase-change-memory-in-smartphones/

Phase Change Random Access Memory (PRAM)

Required writing currents for several techniques dependent upon cell size :





✓Utilise phase change

✓ resistivity : crystalline phase

✓ resistivity : amorphous phase

✓CMOS process compatible

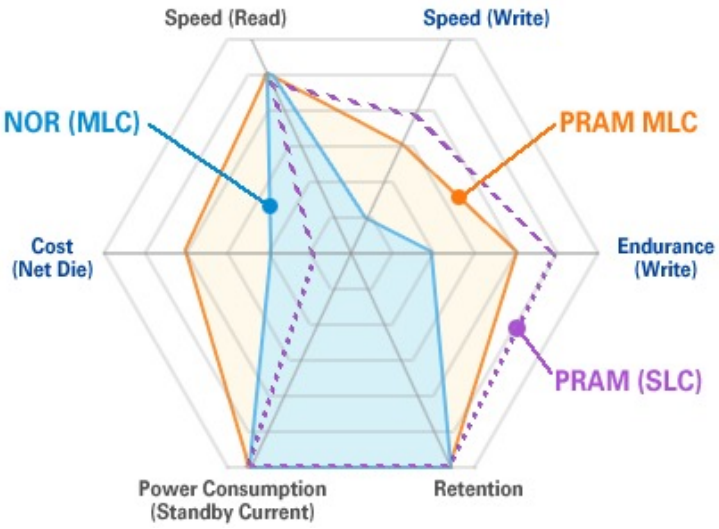
× Rewritability : ~ times

× Destructive read-out

* http://www.wikipedia.org/;
http://nextgenlog.blogspot.com

PRAM Properties

PRAM properties as compared with NOR-flash memory :

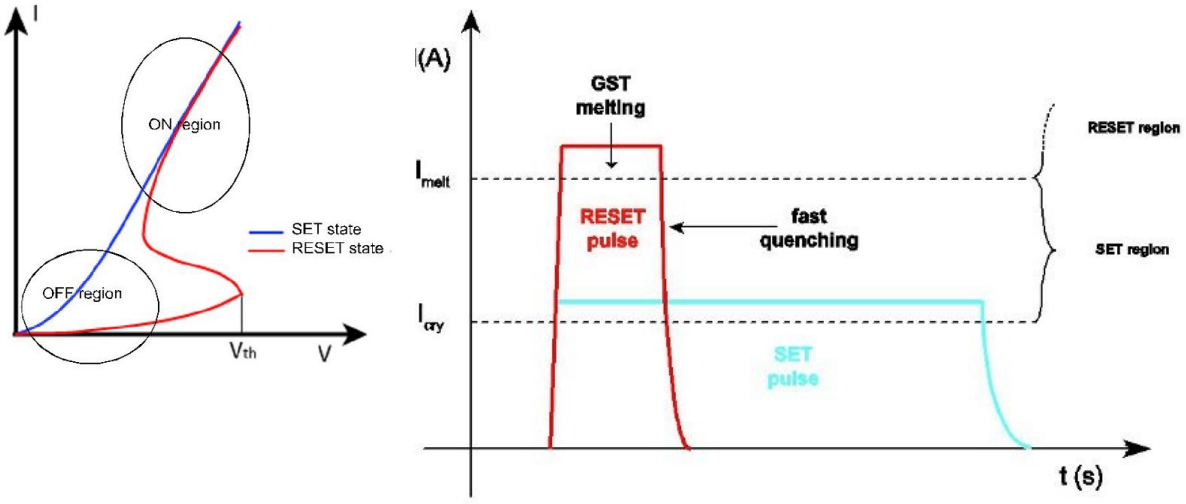


Source : Hynix Marketing

** http://www.hynix.com/mail/newsletter_2009_07/eng/sub02.html

PRAM Operation

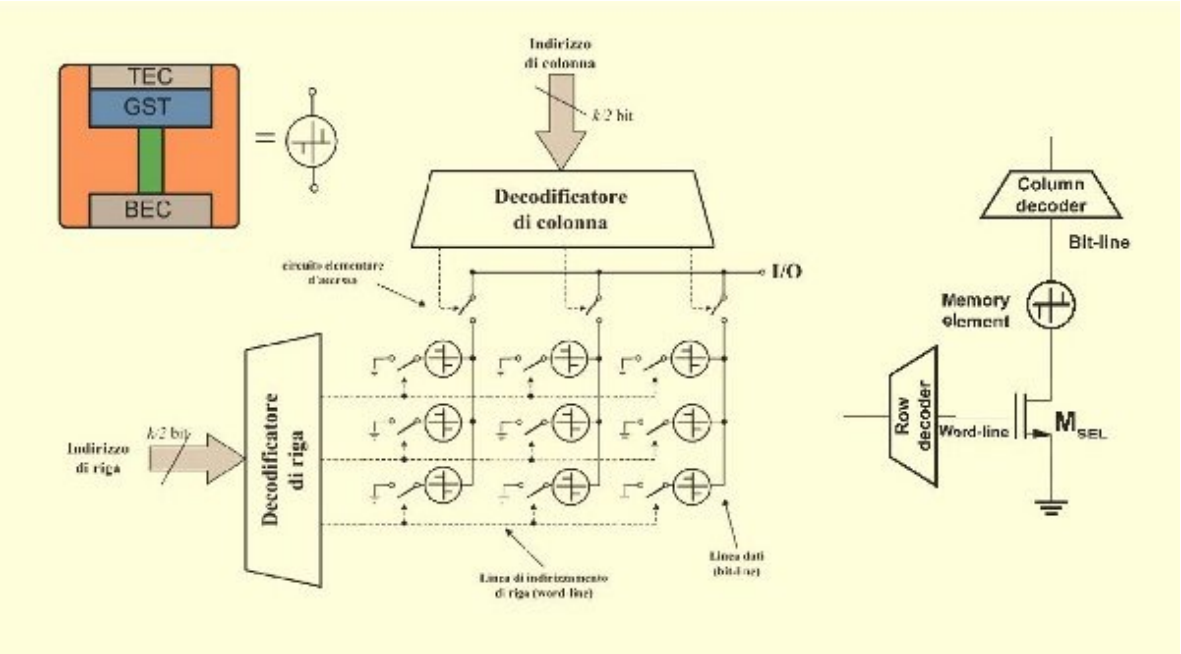
PRAM operation : *



* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/impact-of-technology-scaling-on-phase-change-memory-performance

PRAM Architecture

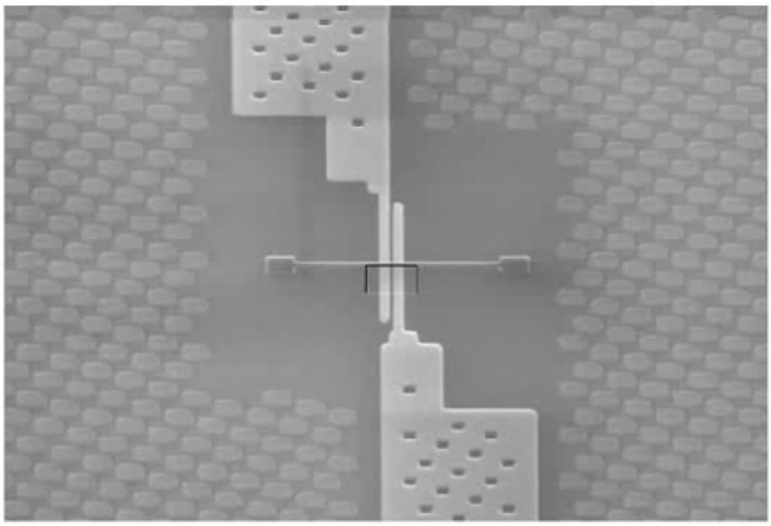
PRAM architecture : *



* http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/impact-of-technology-scaling-on-phase-change-memory-performance

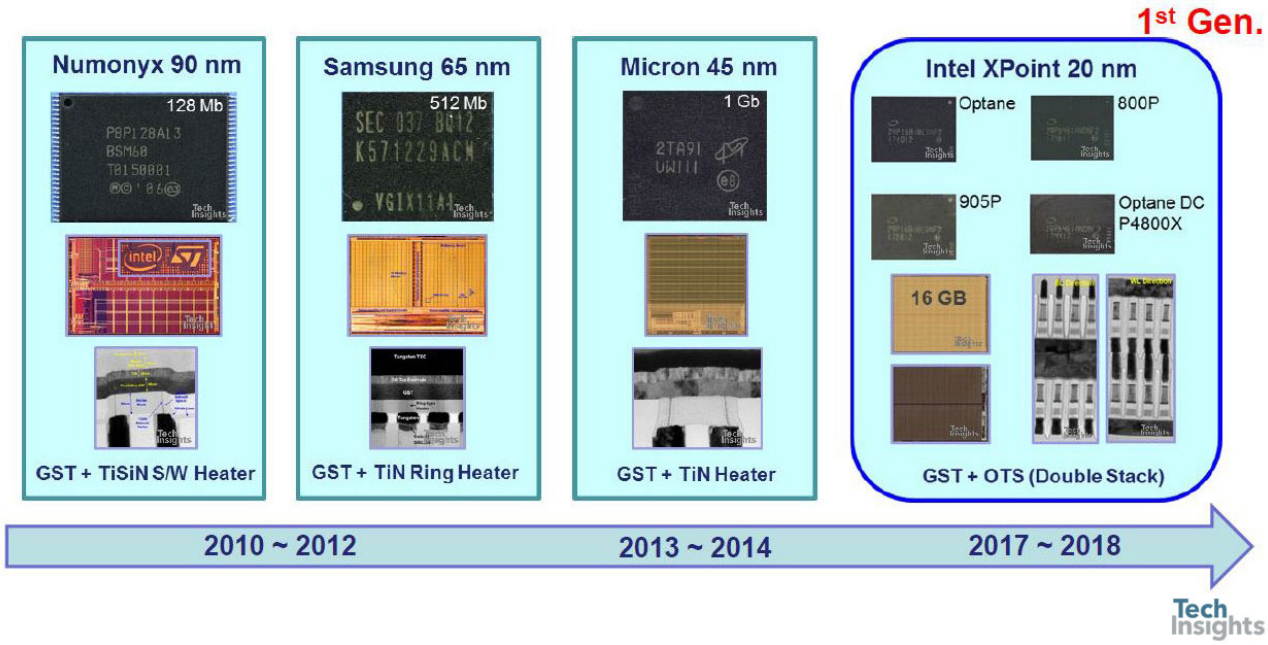
PRAM Operation

IBM MXIC Qimonda Phase Change Memory Joint Project



* https://www.youtube.com/watch?v=n9XoxmPF93c

PRAM Products



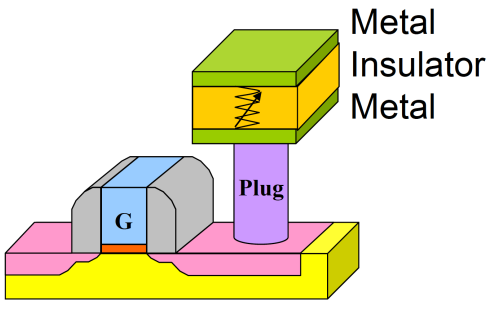
* https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18

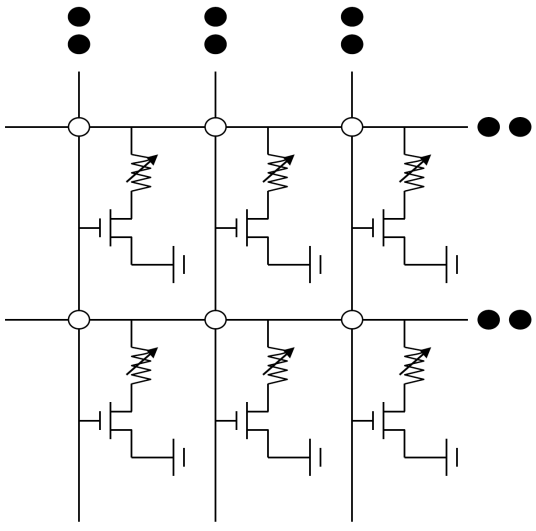
Resistive Random Access Memory (ReRAM)

In 1997, Yoshinori Tokura found colossal magnetoresistance (CMR) :

In 2002, Sharp demonstrated 64-bit ReRAM with $Pr_{0.7}Ca_{0.3}MnO_3$:

Unit cell



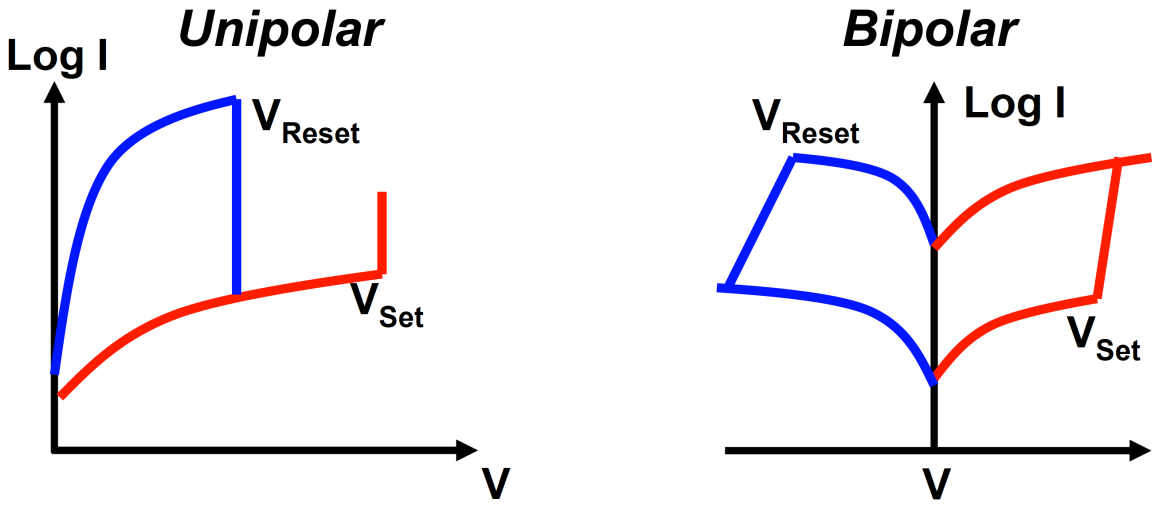


- ✓Utilise large resistivity change
- ✓ endurance : ~ 10^{12}
- ✓Fast switching speed : < 1 ns
- ✓CMOS process compatible

* http://www.cmr.t.u-tokyo.ac.jp/;
** http://phys.nsysu.edu.tw/ezfiles/85/1085/img/588/Oxide-basedResistiveMemoryTechnology_CHLien.pdf

ReRAM Operation

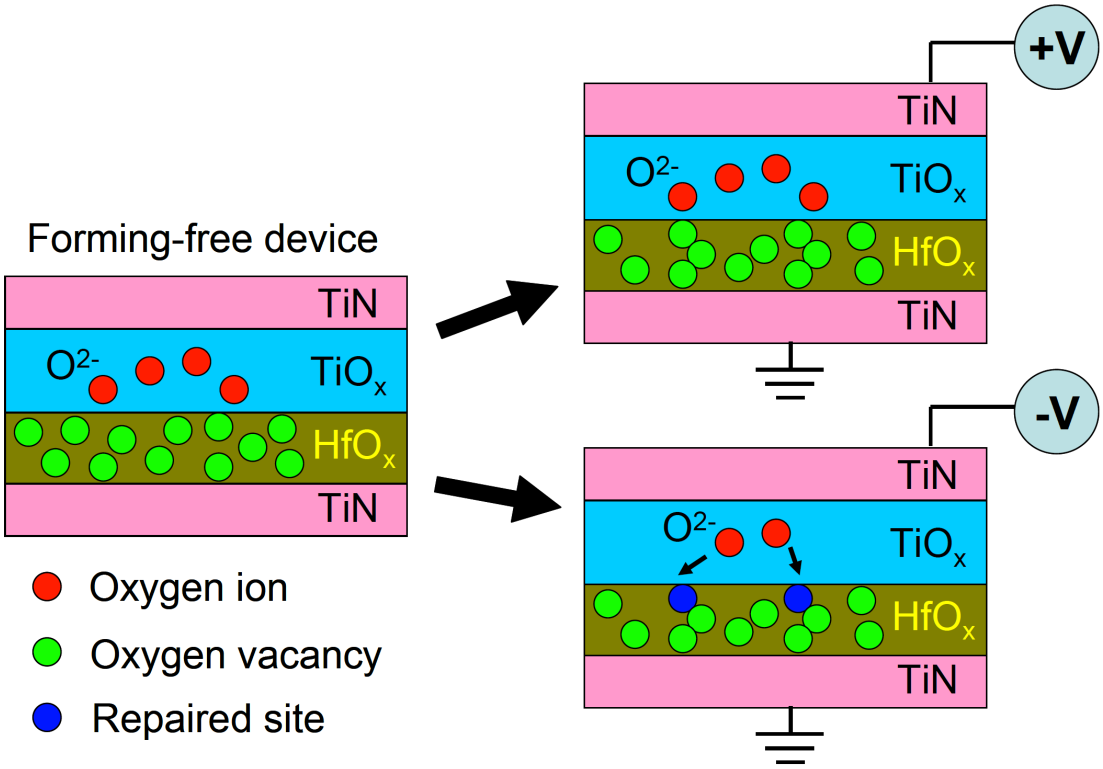
Unipolar / bipolar operations : *



** http://phys.nsysu.edu.tw/ezfiles/85/1085/img/588/Oxide-basedResistiveMemoryTechnology_CHLien.pdf

ReRAM Operation Cycle

Oxygen vacancy can be repaired during the operation cycle : *



** http://phys.nsysu.edu.tw/ezfiles/85/1085/img/588/Oxide-basedResistiveMemoryTechnology_CHLien.pdf

ReRAM Demonstration

Samsung (2004) : *

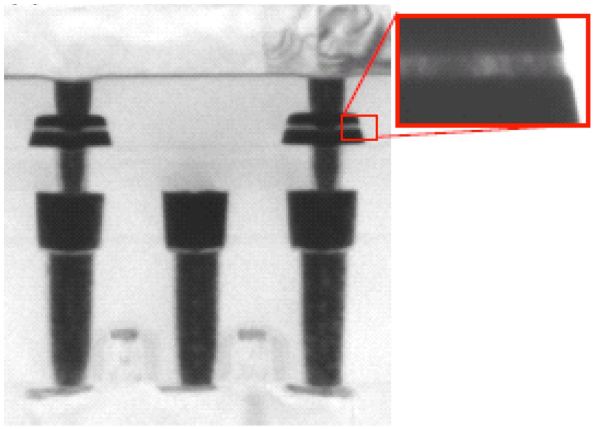
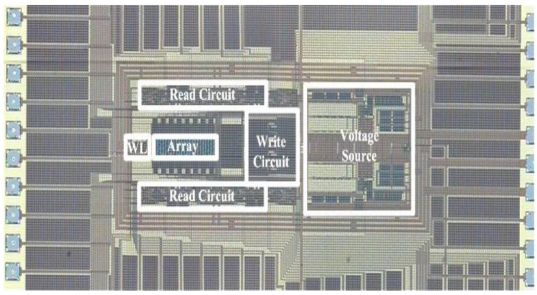
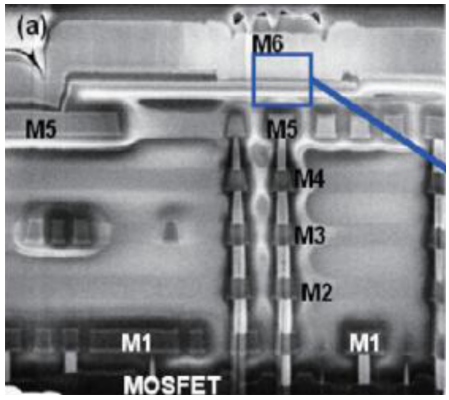
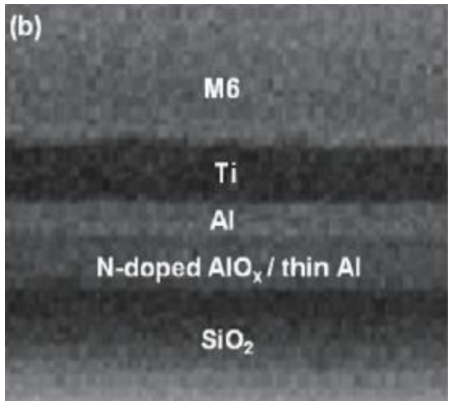


Image of 1kb chip



Stanford (2011) : *



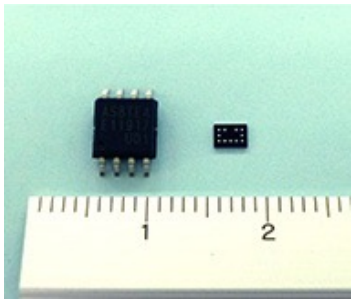


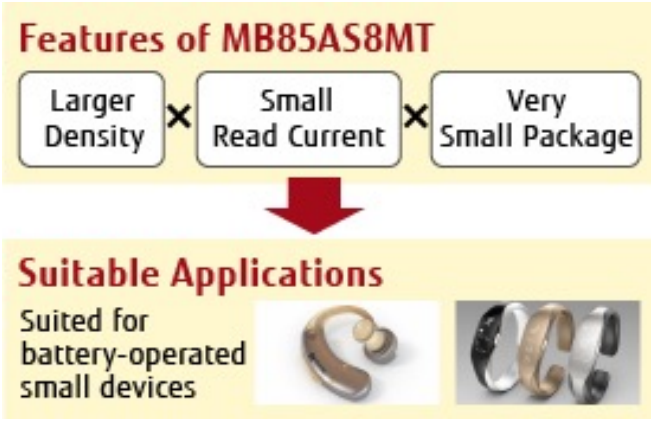
** http://phys.nsysu.edu.tw/ezfiles/85/1085/img/588/Oxide-basedResistiveMemoryTechnology_CHLien.pdf

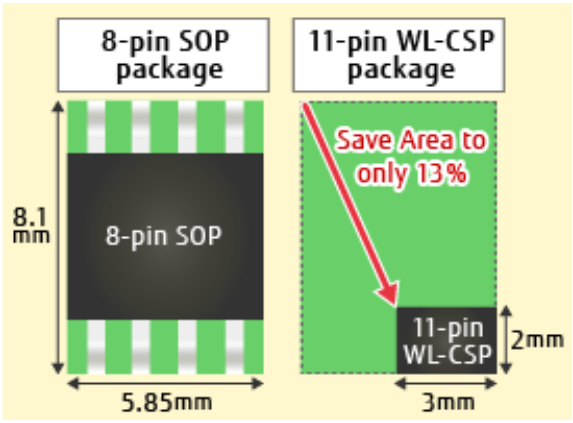
Recent Development

8-Mb ReRAM introduced by Fujitsu and Panasonic :

- Data accessibility at byte by byte
- A small read-out current
  → mA at MHz operation
  → % of that for EEPROM (electrically erasable programmable read-only memory)

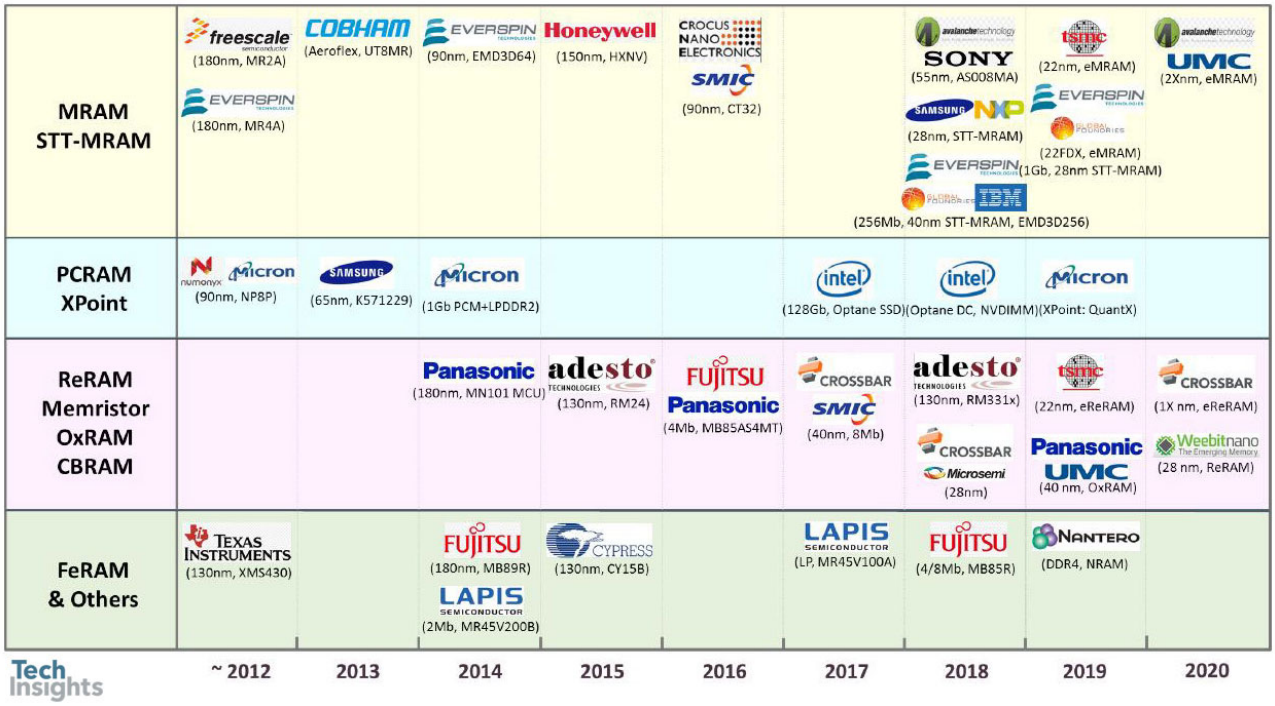






* http://www.fujitsu.com/

Emerging Memory Technologies



* https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18

Memory Comparisons

SRAM
4 Mbit (512 kbit × 8)
10 ns access time (100 MHz)
85 mW active / 7 mW standby
V_{DD} = 2.4 ~ 3.6 V
ISSI
IS61WV5128BLL-10TLI

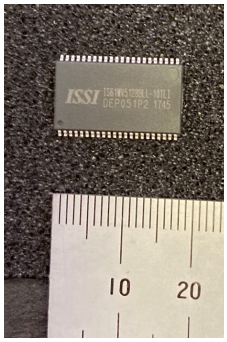
DRAM
4 Gbit (256 Mbit × 16)
1.25 ns access time
(800 MHz)
V_{DD} = 1.5 V
Alliance Memoy
AS4C256M16D3B-12BIN

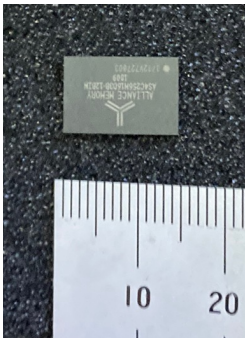
NAND Flash
4 Gbit (512 Mbit × 8)
25 ns access time (40 MHz)

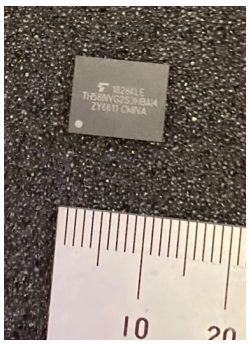
V_{DD} = 2.7 ~ 3.6 V
Toshiba (now Kioxia)
TH58NVG2S3HBAI4

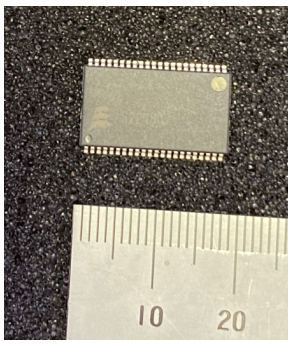
MRAM
16 Mbit
35 ns access time (28.6 MHz)

V_{DD} = -0.5 ~ 4.0 V
Everspin
MR4A08BCYS35









* https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18