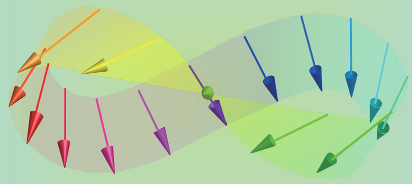
Information Storage and Spintronics 12



Atsufumi Hirohata

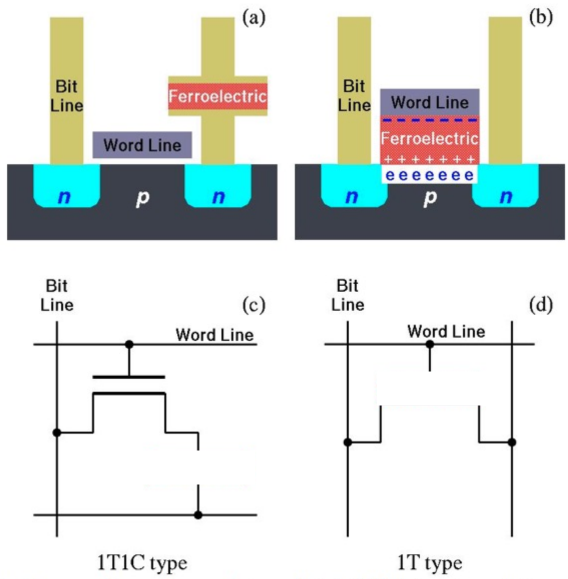
Department of Electronic Engineering

THE UNIVERSITY of York

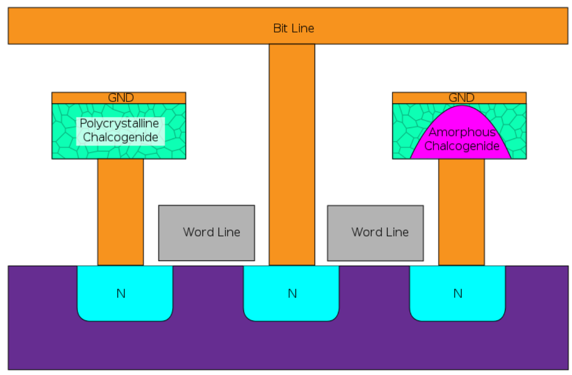
14:00 Thursday, 10/November/2022 (SLB 101)

Quick Review over the Last Lecture

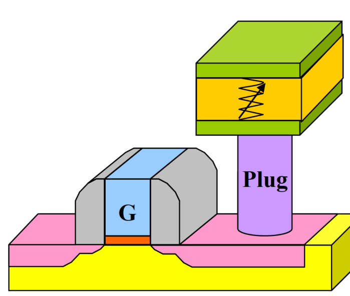
FeRAM :



PRAM :



ReRAM :



* http://loto.sourceforge.net/feram/doc/film.xhtml;
** http://www.wikipedia.org/;
*** http://phys.nsysu.edu.tw/ezfiles/85/1085/img/588/Oxide-basedResistiveMemoryTechnology_CHLien.pdf

12 Spintronic Devices

- Magnetotransport
- Spin generation
- Electrical spin generation
- Giant magnetoresistance
- Tunnelling magnetoresistance
- Current-induced magnetisation reversal

Magnetotransport - Magnetism + Electronics

By taking advantages from both magnetism and semiconductor physics,

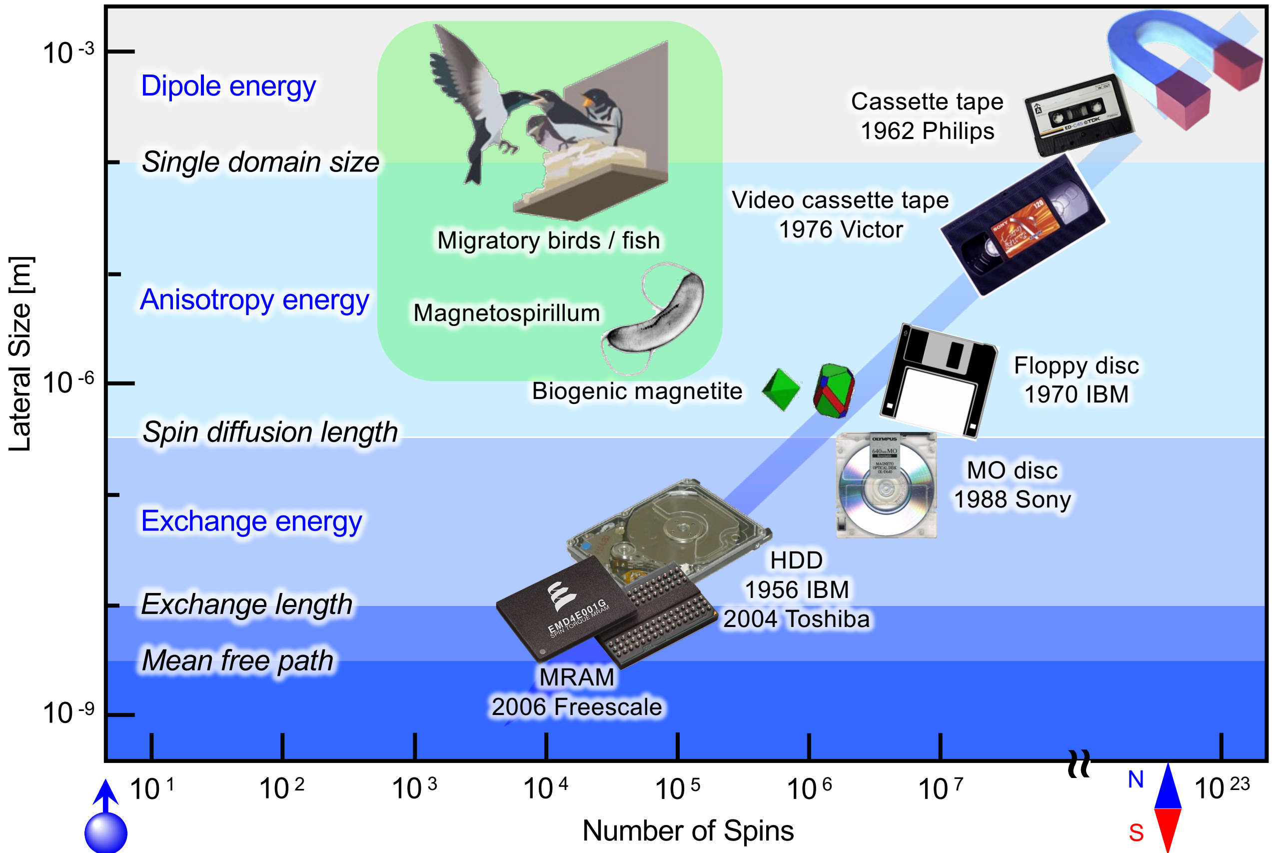
Magnetism

- ✓ Atomically smooth surface / interface
- ✓ Spin diffusion length (~)
- ✓ Low resistivity (Ω•m)
- ✓ Spin polarisation
- ✓ Magnetically anisotropic

Semiconductor physics

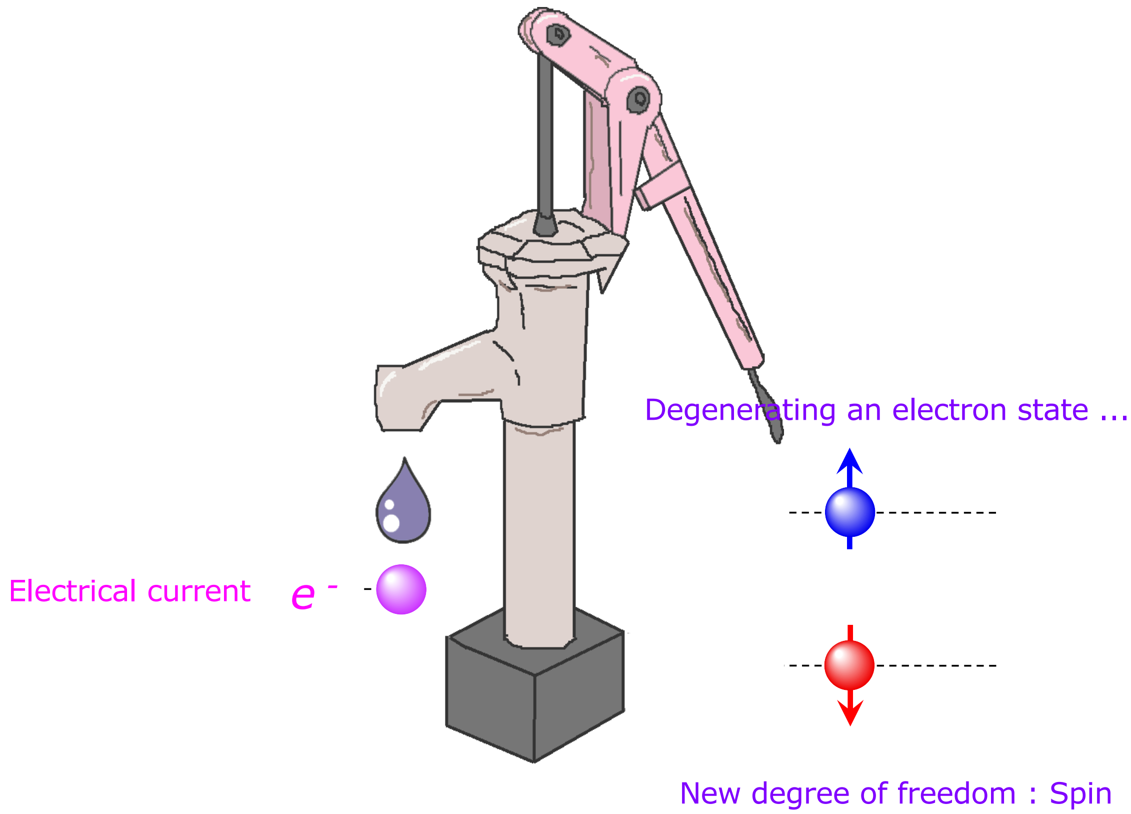
- ✗ Depletion layer ( )
- ✗ Spin diffusion length (~)
- ✓ Variable resistivity (Ω•m)
- ✓ Doping (atomic engineering)
- ✗ Isotropic

Go into Nano-Scale

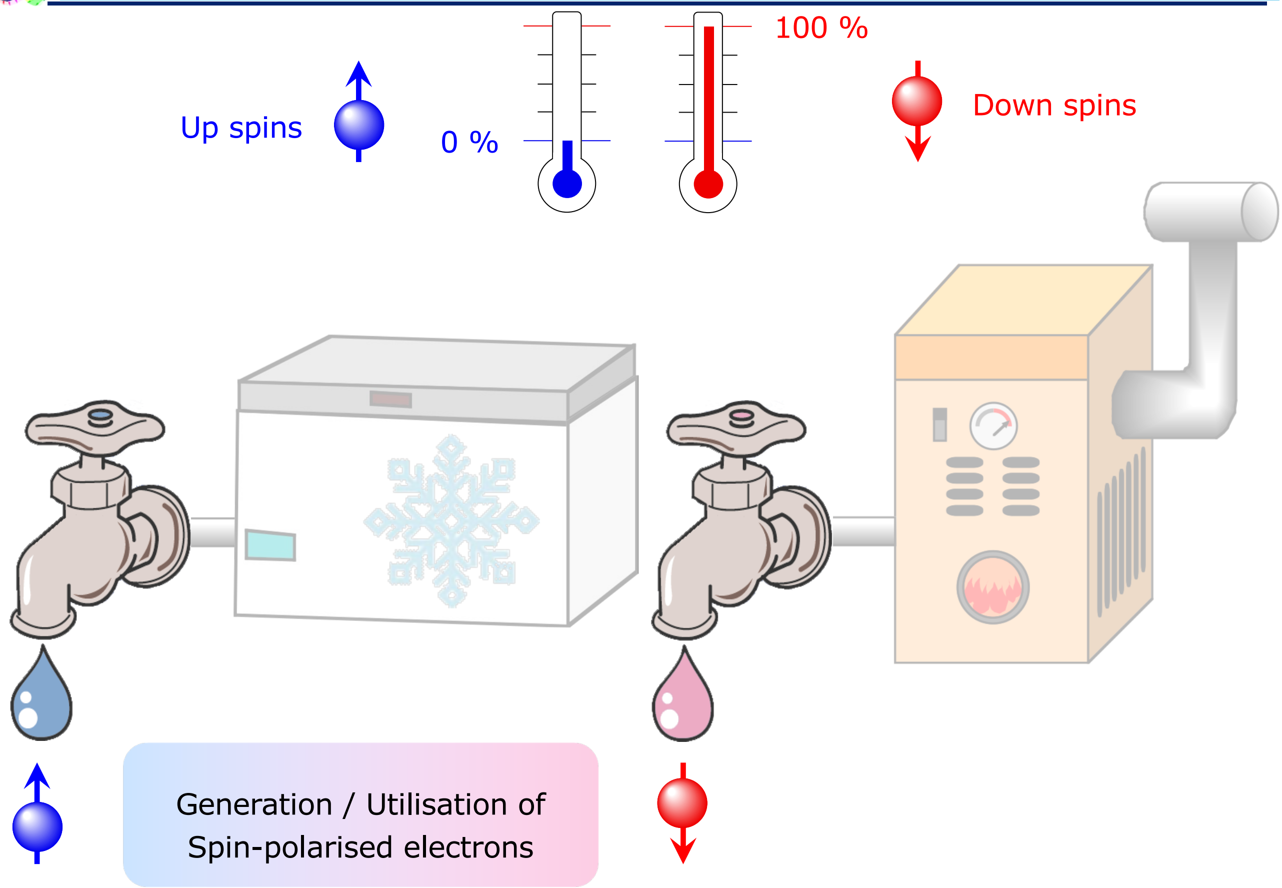


* A. Hirohata and K. Takanashi, *J. Phys. D: Appl. Phys.* **47**, 1930001 (2014).

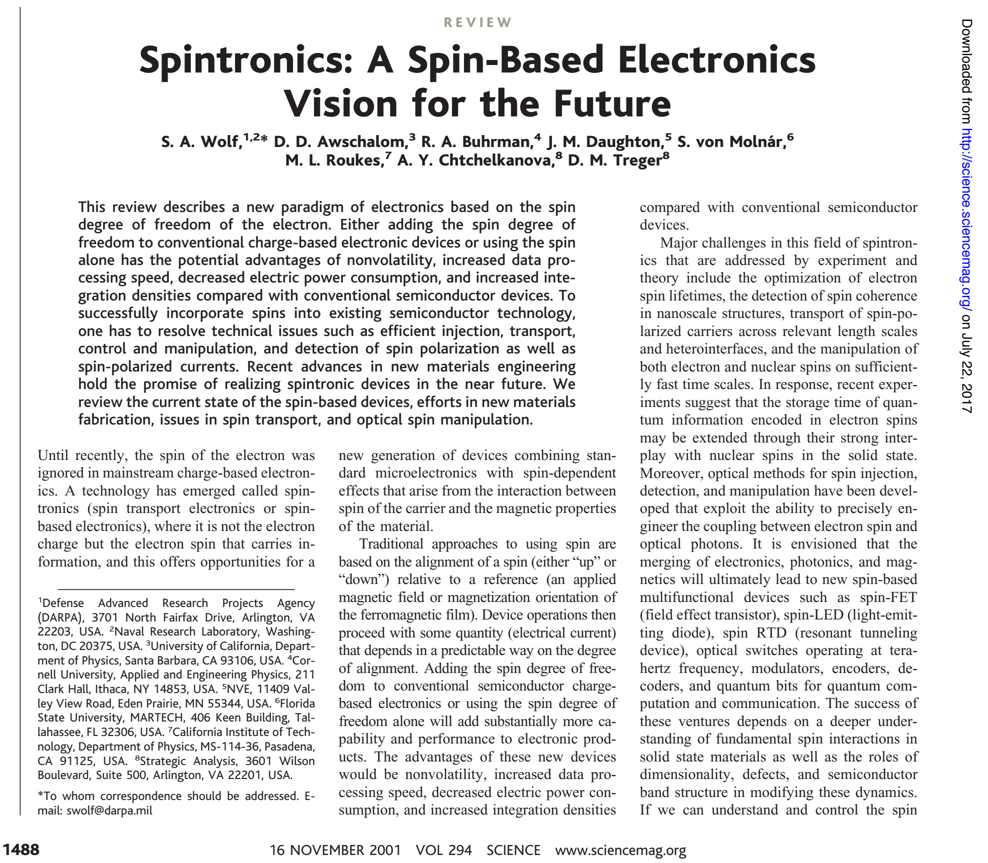
Conventional Electronics



Magnetoelectronics



Rebranding ...



REVIEW

Spintronics: A Spin-Based Electronics Vision for the Future

S. A. Wolf,[1,2]* D. D. Awschalom,[3] R. A. Buhrman,[4] J. M. Daughton,[5] S. von Molnár,[6] M. L. Roukes,[7] A. Y. Chtchelkanova,[8] D. M. Treger[8]

This review describes a new paradigm of electronics based on the spin degree of freedom of the electron. Either adding the spin degree of freedom to conventional charge-based electronic devices or using the spin alone has the potential advantages of nonvolatility, increased data processing speed, decreased electric power consumption, and increased integration densities compared with conventional semiconductor devices. To successfully incorporate spins into existing semiconductor technology, one has to resolve technical issues such as efficient injection, transport, control and manipulation, and detection of spin polarization as well as spin-polarized currents. Recent advances in new materials engineering hold the promise of realizing spintronic devices in the near future. We review the current state of the spin-based devices, efforts in new materials fabrication, issues in spin transport, and optical spin manipulation.

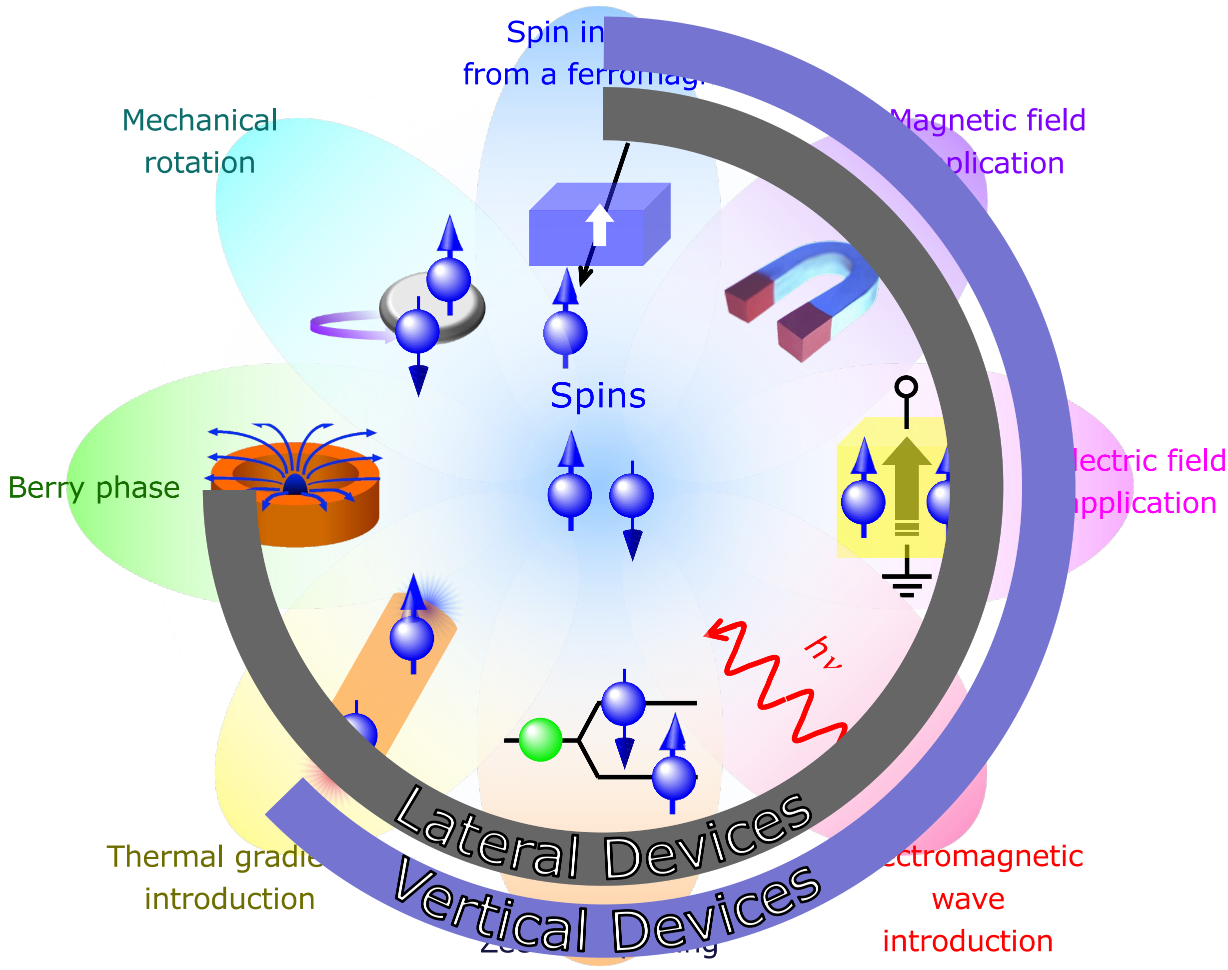
Until recently, the spin of the electron was ignored in mainstream charge-based electronics. A technology has emerged called spintronics (spin transport electronics or spin-based electronics), where it is not the electron charge but the electron spin that carries information, and this offers opportunities for a new generation of devices combining standard microelectronics with spin-dependent effects that arise from the interaction between spin of the carrier and the magnetic properties of the material.

Traditional approaches to using spin are based on the alignment of a spin (either "up" or "down") relative to a reference (an applied magnetic field or magnetization orientation of the ferromagnetic film). Device operations then proceed with some quantity (electrical current) that depends in a predictable way on the degree of alignment. Adding the spin degree of freedom to conventional semiconductor charge-based electronics or using the spin degree of freedom alone will add substantially more capability and performance to electronic products. The advantages of these new devices would be nonvolatility, increased data processing speed, decreased electric power consumption, and increased integration densities compared with conventional semiconductor devices.

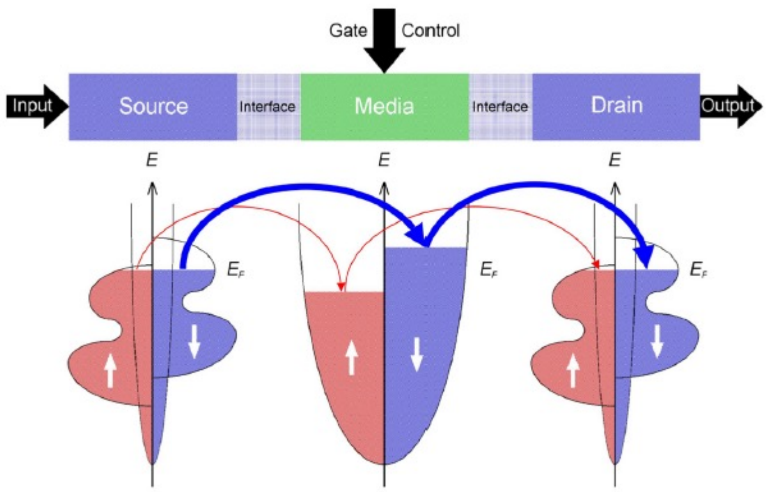
Major challenges in this field of spintronics that are addressed by experiment and theory include the optimization of electron spin lifetimes, the detection of spin coherence in nanoscale structures, transport of spin-polarized carriers across relevant length scales and heterointerfaces, and the manipulation of both electron and nuclear spins on sufficiently fast time scales. In response, recent experiments suggest that the storage time of quantum information encoded in electron spins may be extended through their strong interplay with nuclear spins in the solid state. Moreover, optical methods for spin injection, detection, and manipulation have been developed that exploit the ability to precisely engineer the coupling between electron spin and optical photons. It is envisioned that the merging of electronics, photonics, and magnetics will ultimately lead to new spin-based multifunctional devices such as spin-FET (field effect transistor), spin-LED (light-emitting diode), spin RTD (resonant tunneling device), optical switches operating at terahertz frequency, modulators, encoders, decoders, and quantum bits for quantum computation and communication. The success of these ventures depends on a deeper understanding of fundamental spin interactions in solid state materials as well as the roles of dimensionality, defects, and semiconductor band structure in modifying these dynamics. If we can understand and control the spin

[1]Defense Advanced Research Projects Agency (DARPA), 3701 North Fairfax Drive, Arlington, VA 22203, USA. [2]Naval Research Laboratory, Washington, DC 20375, USA. [3]University of California, Department of Physics, Santa Barbara, CA 93106, USA. [4]Cornell University, Applied and Engineering Physics, 211 Clark Hall, Ithaca, NY 14853, USA. [5]NVE, 11409 Valley View Road, Eden Prairie, MN 55344, USA. [6]Florida State University, MARTECH, 406 Keen Building, Tallahassee, FL 32306, USA. [7]California Institute of Technology, Department of Physics, MS-114-36, Pasadena, CA 91125, USA. [8]Strategic Analysis, 3601 Wilson Boulevard, Suite 500, Arlington, VA 22201, USA.

*To whom correspondence should be addressed. E-mail: swolf@darpa.mil



Nano-Spintronic Devices



	Spin-valve structures	Magnetic tunnel junctions	FM/SC hybrid structures	Organic structures
Effects	GMR	TMR	Diodes	TMR/GMR
Interfaces	Ohmic contacts Diffusive	Tunnel barriers Ballistic	Ohmic/Schottky barriers Diffusive/ballistic (hot electrons)	Ohmic/tunnel barriers Diffusive/ballistic
Spin media	Non-magnetic metals	Tunnel barriers	Semiconductor	Organic materials
Spin coherence	30 nm–1 μm	$\sim$ a few nm	$\leqslant$100 μm	$\sim$ 200 μm
Device applications	Johnson transistors Spin-valve transistors Lateral spin valves	MOS junctions Coulomb blockade structures MRAM Superconducting point contacts Spin RTD Magnetic tunnel transistors SP-STM	FM/2DEG Schottky diodes Spin FET Spin LED Spin RTD	Lateral spin valves

* A. Hirohata and K. Takanashi, *J. Phys. D: Appl. Phys.* 47, 1930001 (2014).

Theoretical Models for GMR

Interlayer exchange coupling model :

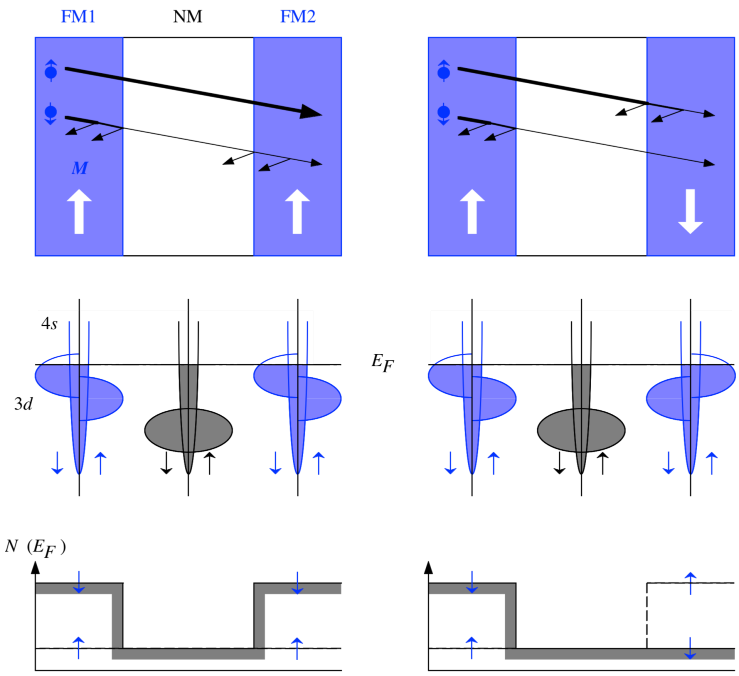
RKKY-like oscillation *

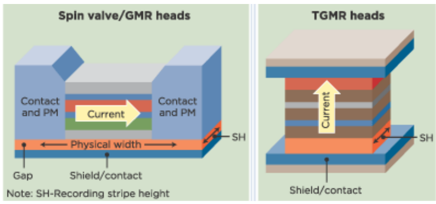
Two current model :

3*d* ferromagnets (FM) carry
- up spin current
- down spin current

independently with different scattering rates at
- the FM layers
- the FM / NM interfaces. **

Current orientation :
- Current in the plane (CIP)
- Current perpendicular to the plane (CPP)



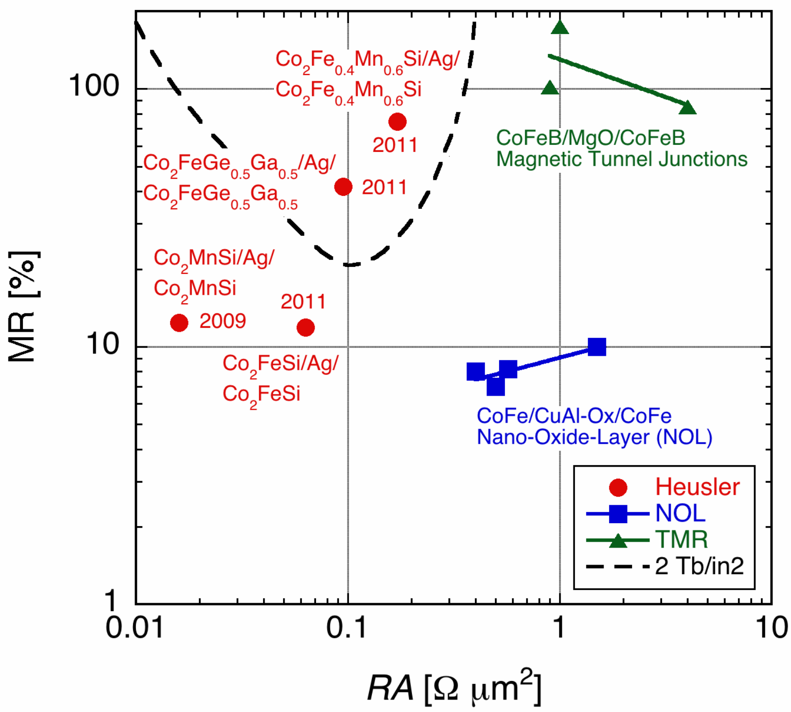


* K. B. Hathaway, *Ultrathin Magnetic Structures II*, B. Heinrich and J. A. C. Bland (Eds.) (Springer, Berlin, 1994), p. 45-72;
** J. Mathon, *Spin Electronics*, M. Ziese and M. J. Thornton (Eds.) (Springer, Berlin, 2001), p. 71-88.

Larger GMR Ratios

For > 2 Tb/in² recording :

Larger GMR ratios and smaller resistance-area product (*RA*) are required.

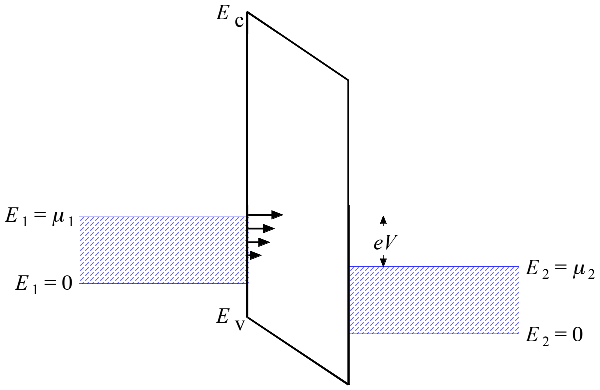


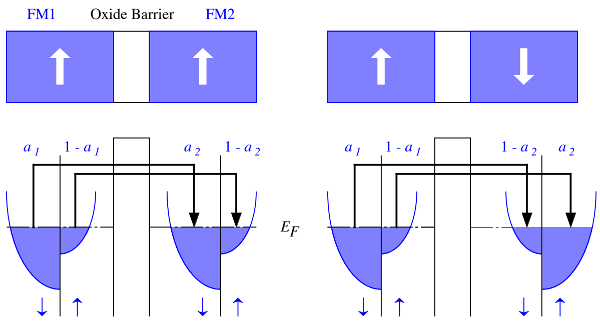
* A. Hirohata *et al.*, *Appl. Phys. A* **111**, 423 (2013).

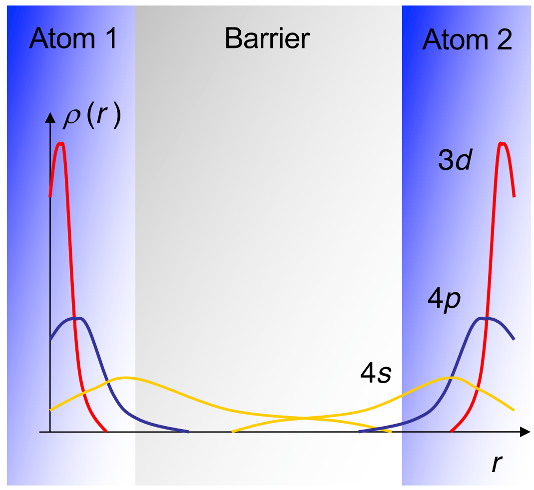
Spin-Dependent Electron Tunneling

Jullière's model :

FM / insulator / FM junctions *







* M. Jullière., *Phys. Rep.* **54A**, 225 (1975).

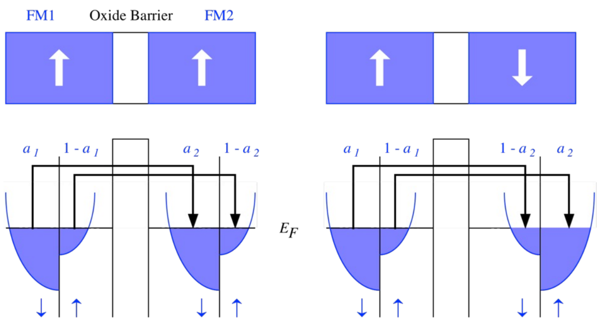
Theoretical Models for TMR

Free electron models :

Juliere's model :

$$\begin{cases} G^{P} \propto a_1 a_2 + (1 - a_1)(1 - a_2) \\ G^{AP} \propto a_1 (1 - a_2) + (1 - a_1) a_2 \end{cases}$$

$$\text{TMR ratio} =$$



Slonczewski's model * :

spin split free electron band

→ for large energy gap in a barrier, spin polarisation :

$$P =$$

WKB approximation **

Transfer Hamiltonian approach

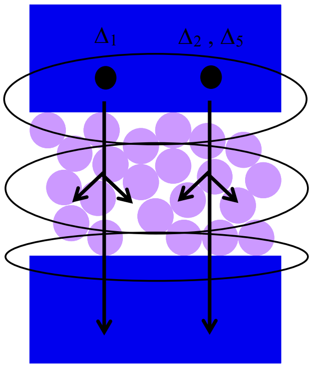
Ab initio calculations

J. C. Slonczewski, *Phys. Rev. B* **39**, 6995 (1989);
** W. F. Brinkman *et al.*, *J. Appl. Phys.* **41**, 1915 (1970).

Improved Tunnel Barriers

Conventional amorphous barriers : *

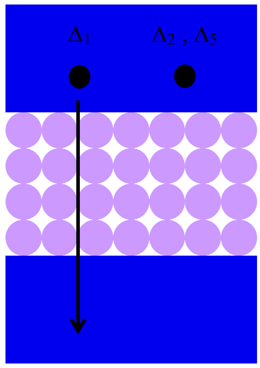
Defects in the barrier



Disorder at the interface :
- FM over-oxidation
- lattice defects

Disorder at the interface :
- FM over-oxidation
- lattice defects
- island growth of the barrier

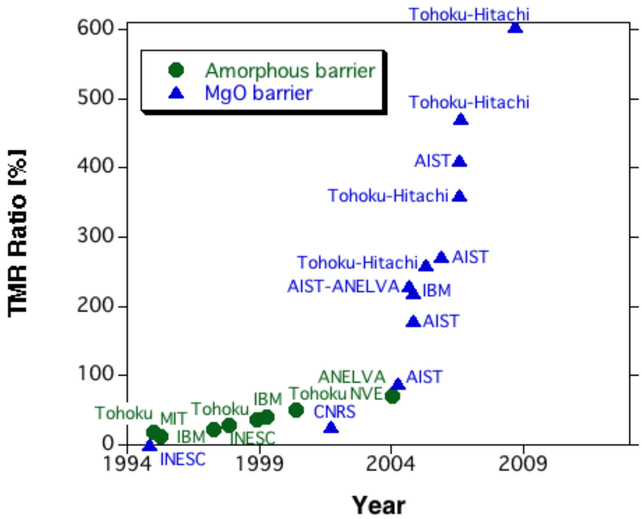
Epitaxial (oriented) barriers : *



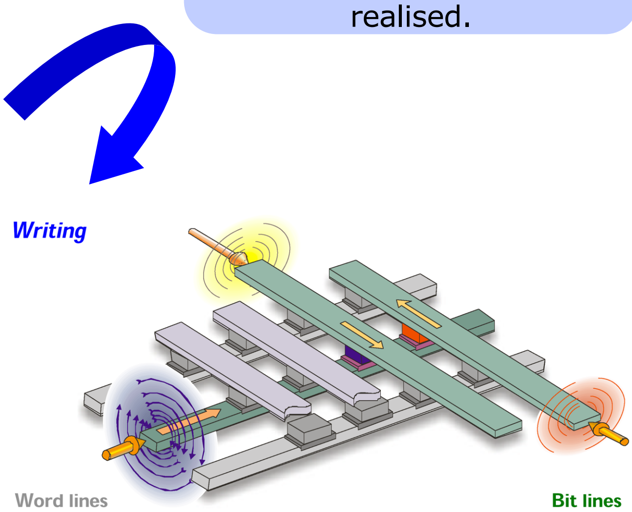
* *After* S. Yuasa *et al.*, *28th Annual Conference on Magnetics*, Sep. 21-24, 2004 (Okinawa, Japan).

TMR for Device Applications

Recent progress in TMR ratios :



> *600 % TMR ratio* has been achieved !
> ↓
> Gbit MRAM can be realised.



NOT following Jullière's model : *

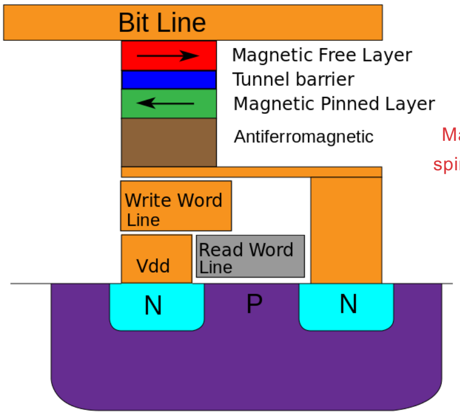
$$\mathrm{TMR} = 2P_1P_2 \,/\, (1 - P_1P_2)$$

* M. Jullière., *Phys. Rep.* **54A**, 225 (1975).

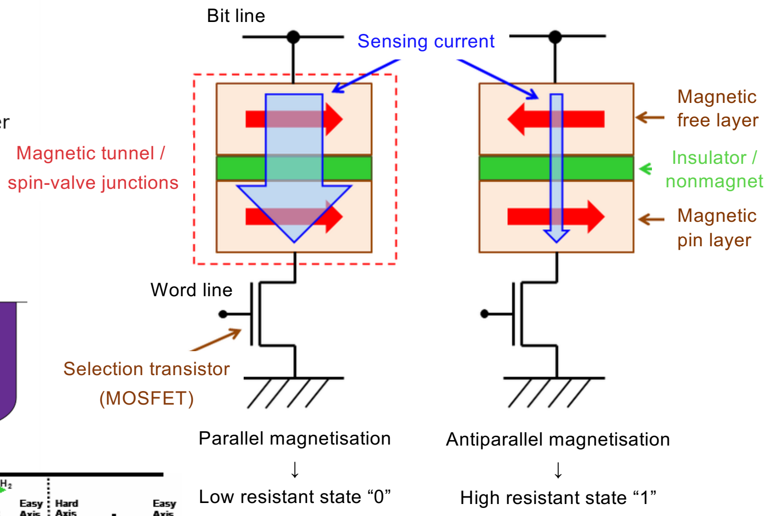
** S. S. P. Parkin, *1st Int'l Sch. on Spintronics and Quantum Info. Tech.*, May 13-15, 2001 (Maui, HI, USA).

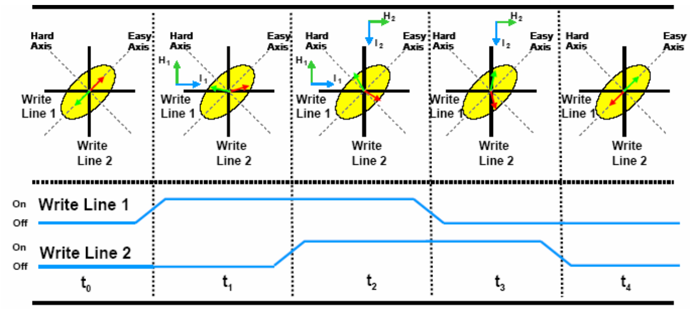
MRAM Cell

MRAM cell structure :



MRAM read-out :

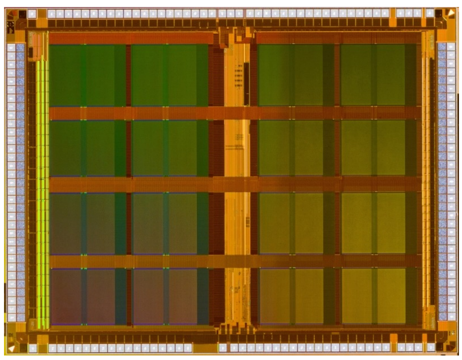


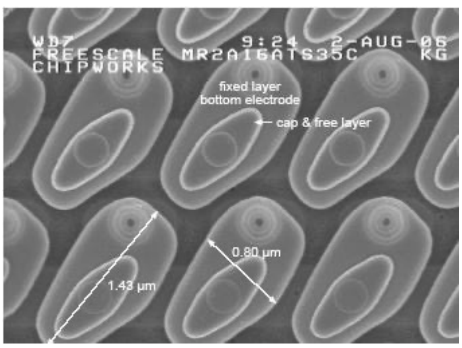


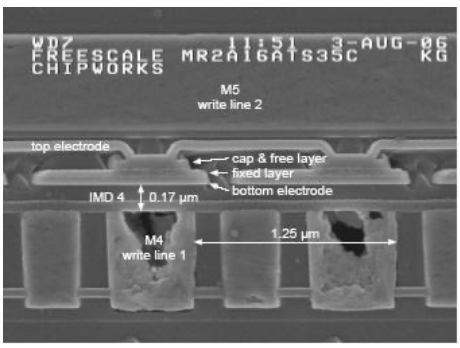
* http://www.wikipedia.org/;
** J. Åkerman *et al.*, in M. Johnson (*Ed.*), *Magnetoelectronics* (Elsevier, Amsterdam, Netherlands, 2004) p. 231-272.

MRAM Products

Freescale (now EverSpin Technologies) 4 Mbit MRAM :

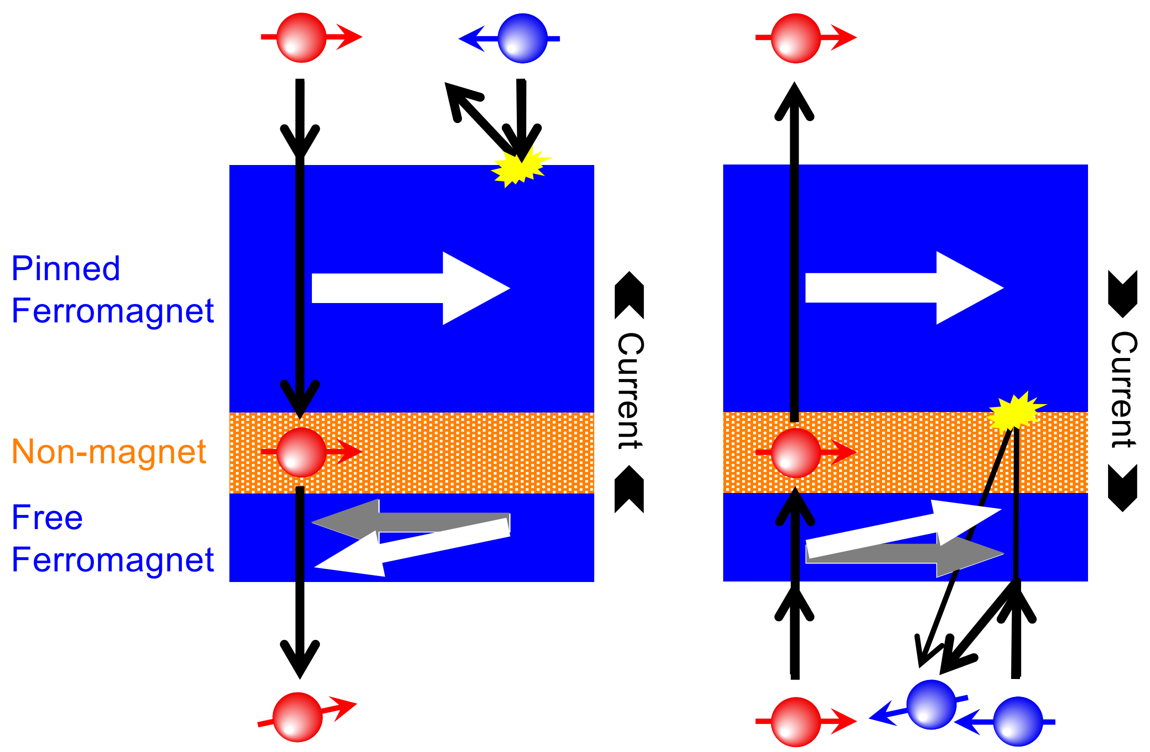






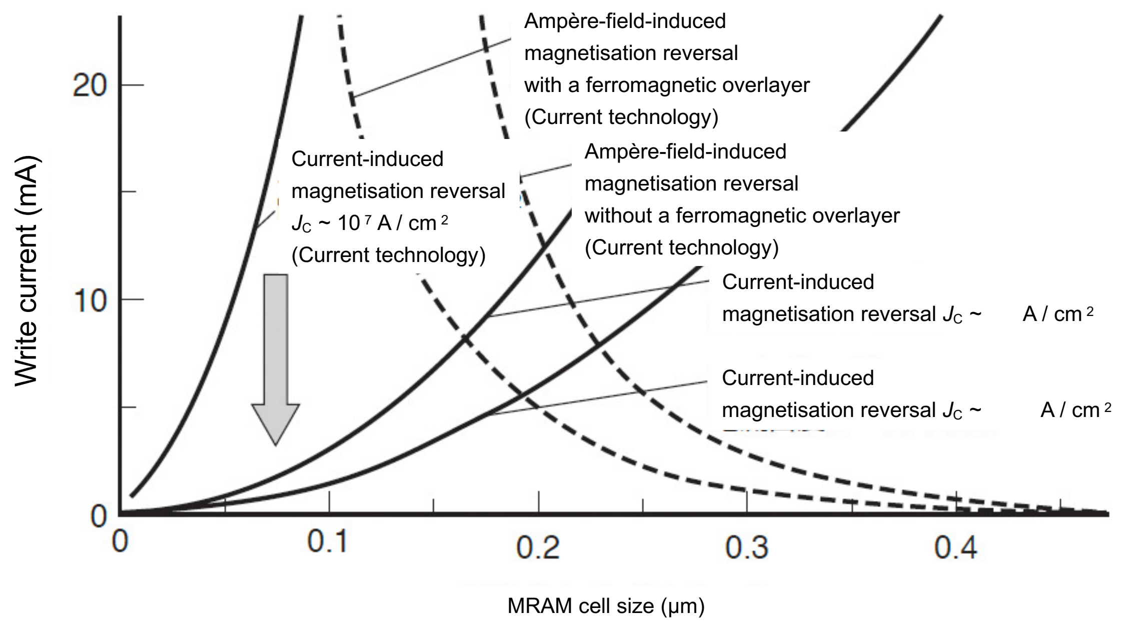
* http://www.freescale.com/;
** http://www.chipworks.com/blogs.aspx?id=2514

Current-Induced Magnetisation Switching



Improved MRAM Operation (Spin RAM)

Required writing currents for several techniques dependent upon cell size :



* S. Nakamura, Y. Saito and H. Morise, *Toshiba Rev.* **61**, 40 (2006).

Advantages of MRAM / Spin RAM

	Spin RAM	MRAM	FLASH		DRAM		FeRAM	SRAM
Rules	32 nm	90 nm	32 nm	90 nm	45 nm	90 nm		90 nm
Non-volatility	Y	Y	Y	Y	N	N	Y	N
Read time	~1 ns	300 ns (GMR) <60 ns (TMR)	10–50 ns	10–50 ns	10 ns	10 ns	100–200 ns	1.1 ns
Write time	~1 ns	<10 ns	0.1–100 ms	0.1–100 ms	10 ns	10 ns	~100 ns	1.1 ns
Repetition	$>10^{15}$	$>10^{15}$	$>10^{6}$	$>10^{6}$	$>10^{15}$	$>10^{15}$	10^{9}–10^{12}	$>10^{15}$
Cell size	0.01 μm^2 5 Gb cm^{-2}*	0.25 μm^2 256 Mb cm^{-2}	0.02 μm^2 2.5 Gb cm^{-2}*	0.1 μm^2 512 Mb cm^{-2}		0.25 μm^2 256 Mb cm^{-2}		1–1.3 μm^2 64 Mb cm^{-2}
Cell density	6 F^2	27 F^2		4 F^2	6 F^2	8 F^2	8 F^2	92 F^2
Chip capacity		>1 Gb		>1 Gb			<10 Mb	
Program energy per bit		120 pJ	10 nJ	30–120 nJ		5 pJ + refresh		5 pJ
Soft error hardness		Y		Y		Y	Y	N
Process cost		RT process		Lower bit cost			HT process	

Note: * represents target values.

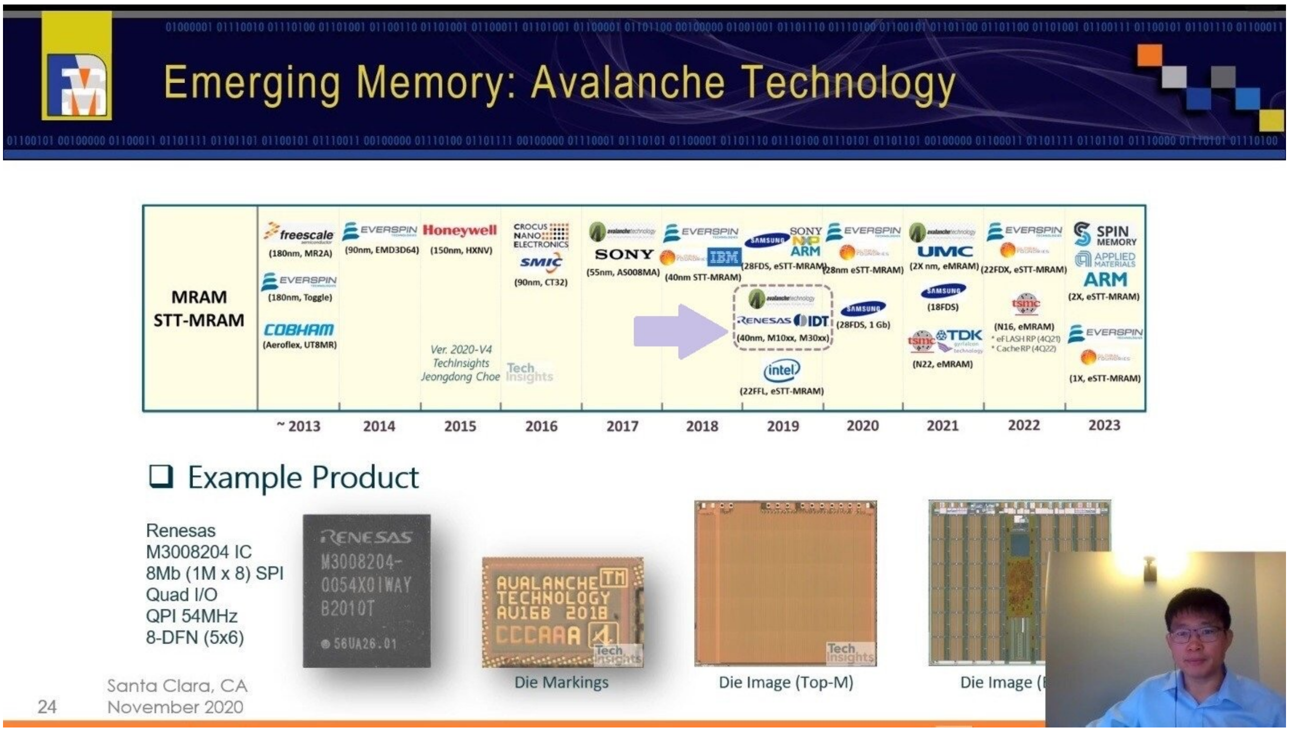
S Azzawi et al 2017 J. Phys. D: Appl. Phys. 50 473001

* A. Hirohata and K. Takanashi, *J. Phys. D: Appl. Phys.* **47**, 1930001 (2014).

MRAM Operation

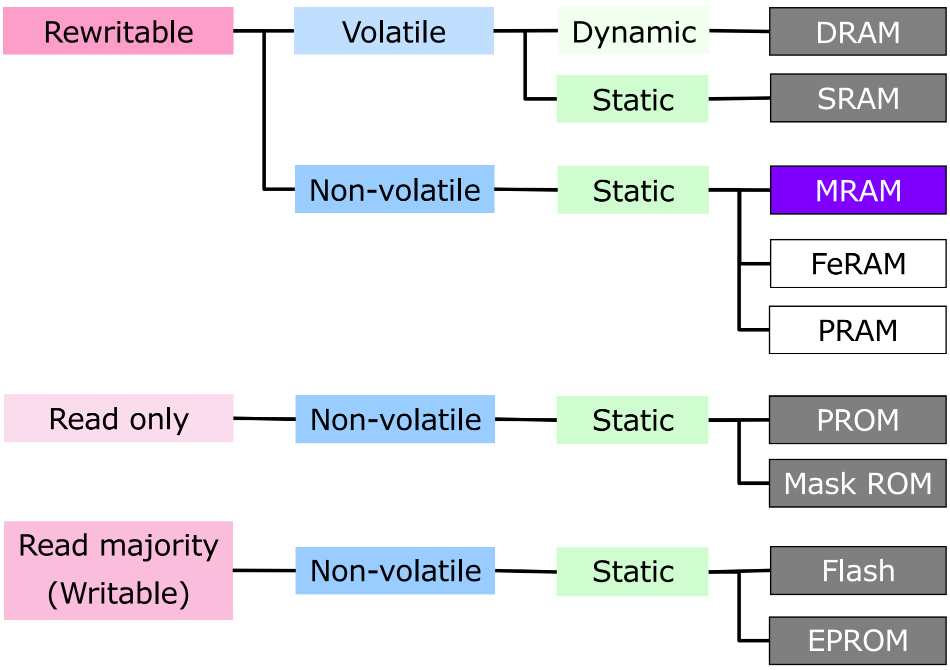
* https://www.youtube.com/watch?v=VRJ7xYPMfGA

Development of MRAM



* https://eetimes.jp/ee/articles/2104/23/news028_2.html

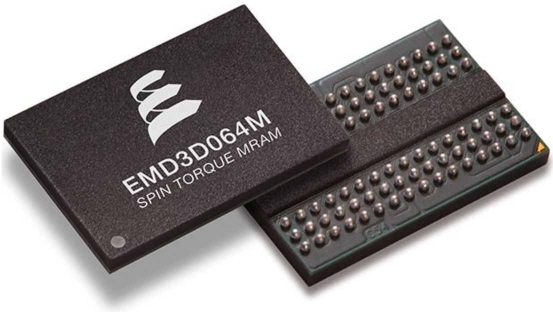
Memory Types



* http://www.semiconductorjapan.net/serial/lesson/12.html

STT-MRAM Products

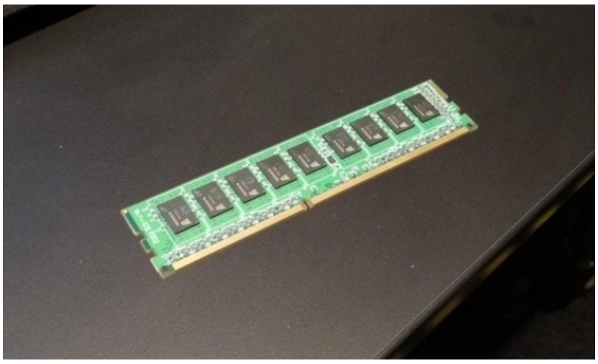
In 2012, EverSpin Technologies introduced 64 Mbit MRAM :



500x Performance…

	NAND	MRAM
Density	64Gb	1Gb
Power	80mW	400mW
4kB Write IOPS	800	400k
Cost/GB	1	50

…at only 5x Power



* http://www.everspin.com/

STT-MRAM Advantages 1

ST-MRAM *Delivering 10x better Price/Performance*

Cloud Storage Needs:

- More content & users, instant access
- Better response times from storage
- Predictable balanced performance

Nanosecond-class MRAM Storage

NAND SSD

500x Performance…

	NAND	MRAM
Density	64Gb	1Gb
Latency	50us	45ns
4kB Write IOPS	800	400k
Cost/GB	1	50

…at only 50x Cost/GB

MRAM SSD

EVERSPIN TECHNOLOGIES The MRAM Company

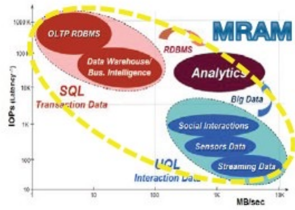
* http://www.everspin.com/

STT-MRAM Advantages 2

ST-MRAM *Delivering 100x Power/Performance*

Data Center needs:

- Number of servers & CPU cores exploding
- Better bandwidth & IOPS to handle Big Data
- More performance @ less power to scale up



High Performance, Power-Efficient MRAM Storage

NAND SSD

500x Performance…

	NAND	MRAM
Density	64Gb	1Gb
Power	80mW	400mW
4kB Write IOPS	800	400k
Cost/GB	1	50

…at only 5x Power

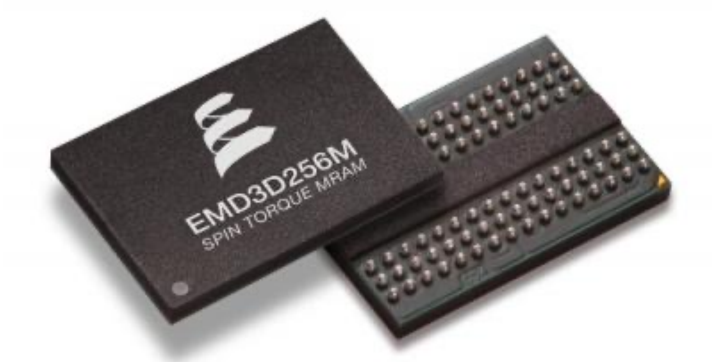
MRAM SSD

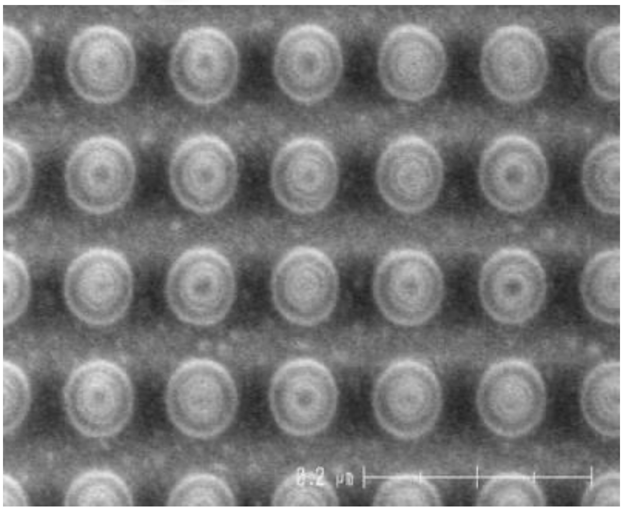
EVERSPIN TECHNOLOGIES The MRAM Company

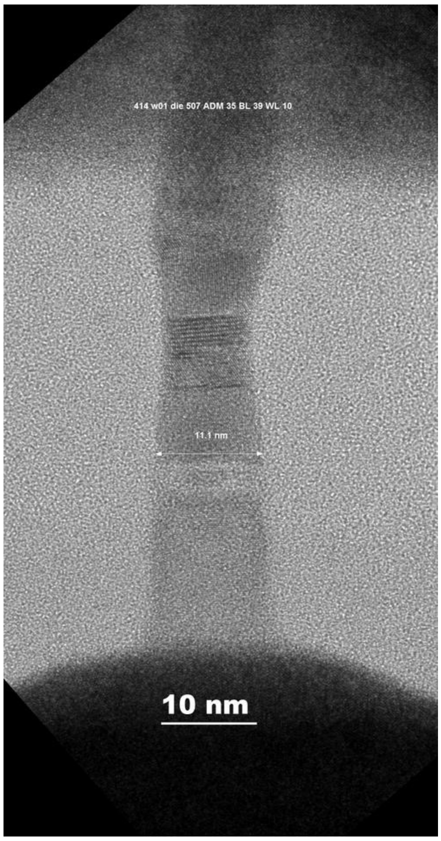
14

* http://www.everspin.com/

Latest Spin RAM

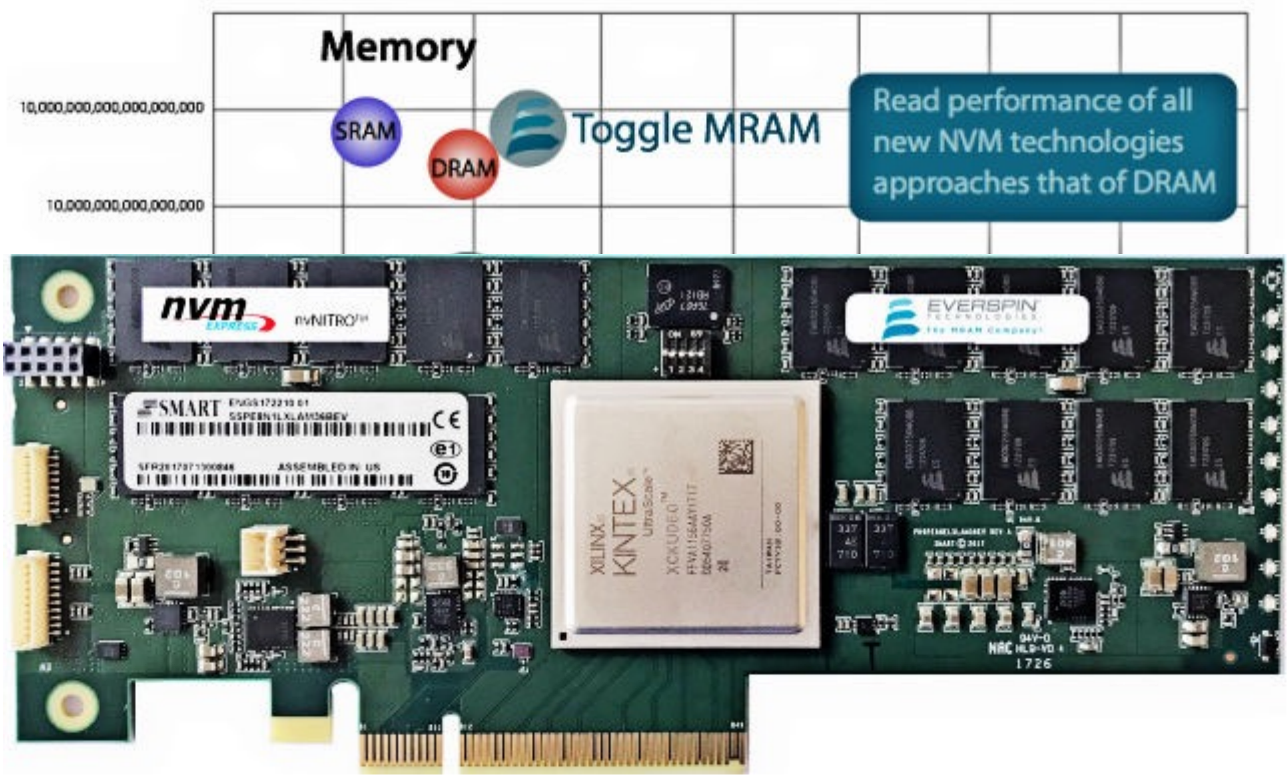






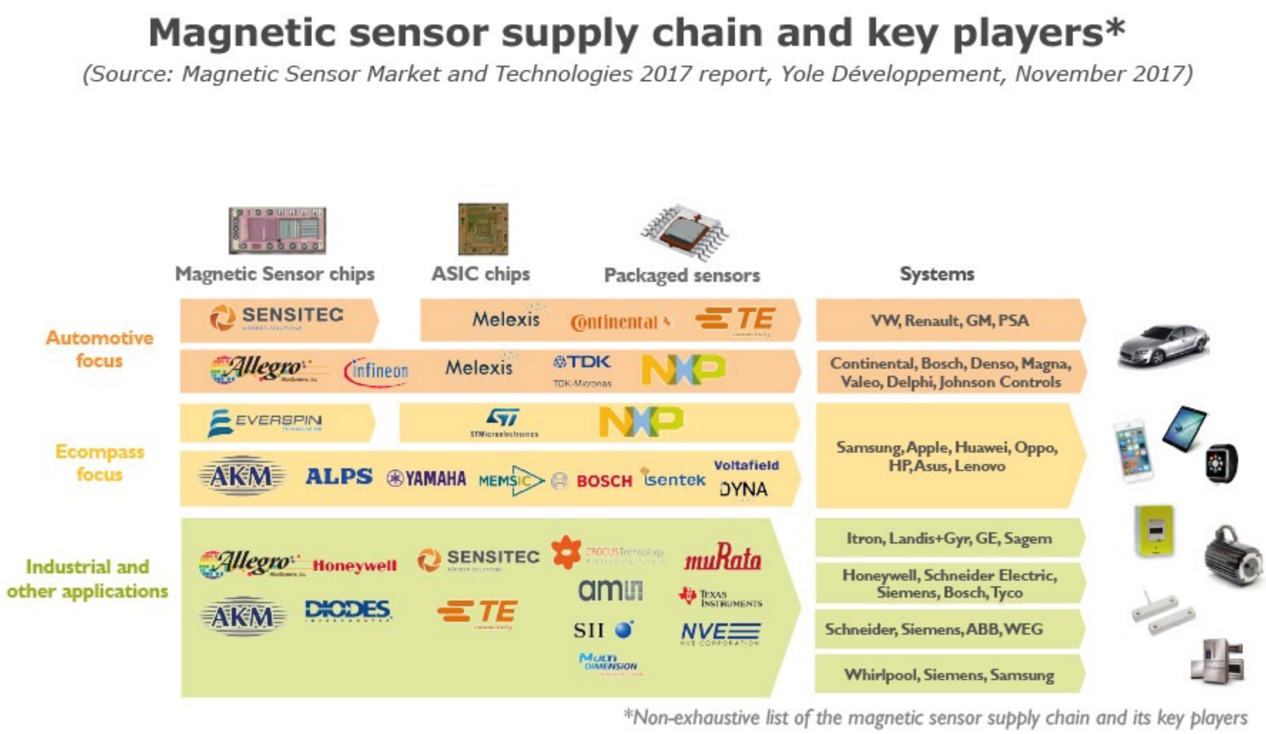
* News from EverSpin, IBM and Toshiba.

MRAM for SRAM / DRAM Replacement



* https://forums.xilinx.com/t5/Xcell-Daily-Blog/Everspin-s-new-MRAM-based-nvNITRO-NVMe-card-delivers-Optane/ba-p/785194

MRAM Manufacturers



* https://www.i-micronews.com/

MRAM Applications