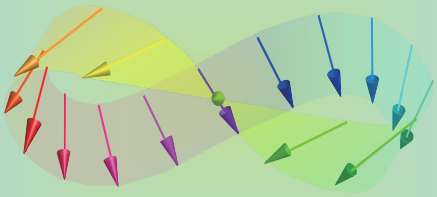
Information Storage and Spintronics 14



Atsufumi Hirohata

Department of Electronic Engineering

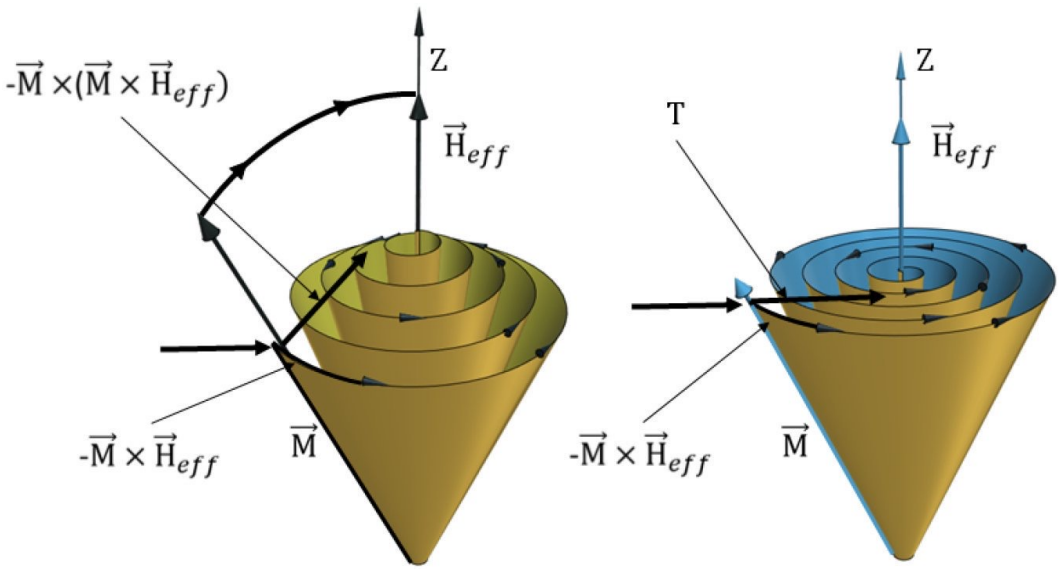
THE UNIVERSITY of York

15:00 Monday, 14/November/2022 (SLB 004)

Quick Review over the Last Lecture

Landau-Lifschits-Gilbert equation : *

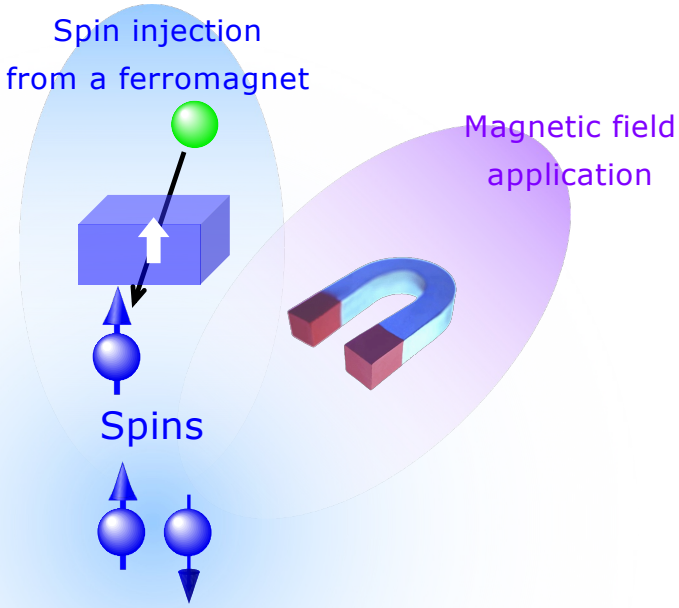
$$\frac{\partial m}{\partial t} = -\gamma m \times H_{\mathrm{eff}} + \alpha m \times \frac{\partial m}{\partial t}$$



* A. Hirohata (Guest Editor), *J. Phys. D: Appl. Phys.* 44, 380301 (2011).

14 Domain Wall Memories

- Domain wall energy
- Racetrack memory
- Operation speed
- Walker's breakdown
- Three-terminal memory



Domain wall energy can be determined as follows : *

$$E_{\mathrm{DW}} = \int_{-w/2}^{+w/2} \{E_{\mathrm{a}}(x) + E_{\mathrm{ex}}(x)\} dx$$

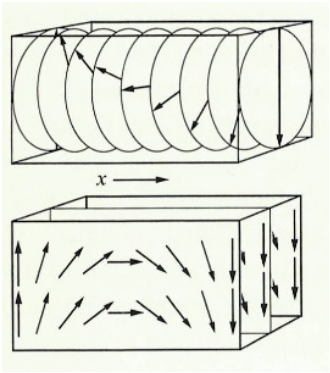
where E_{a} : the magnetic anisotropy energy, E_{ex} : the magnetic exchange energy and w : a domain wall width.

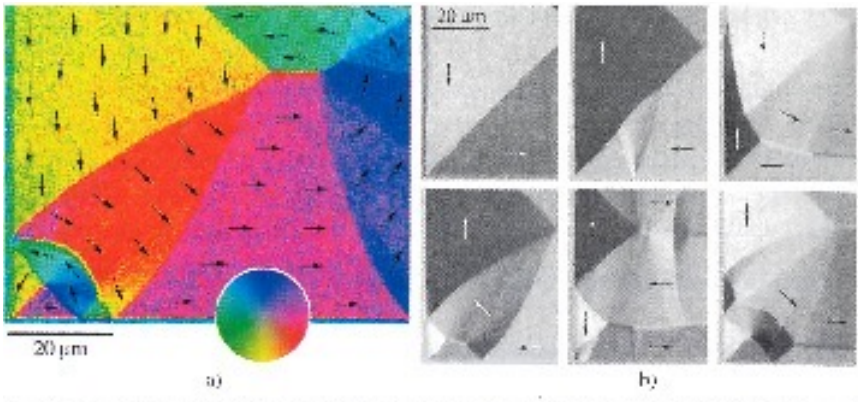
For a uniaxially anisotropic sample with the uniaxial anisotropy K_{u} and the exchange stiffness constant A_{ex}, a domain wall width can be calculated as

$$w =$$

Here, the domain wall energy becomes

$$E_{\mathrm{DW}} =$$

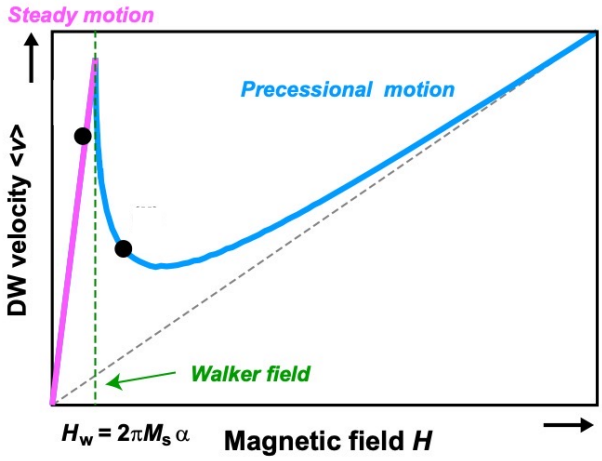


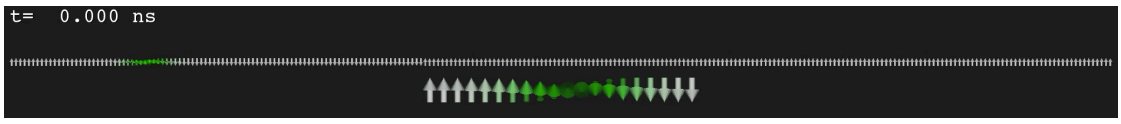


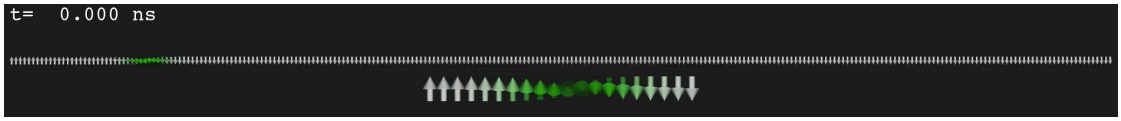
* A. Hubert and R. Schäfer, *Magnetic Domains* (Springer, Berlin, 2000).

Domain Wall Motion by a Magnetic Field

Domain wall can be moved by an application of a magnetic field : *







Walker breakdown : *

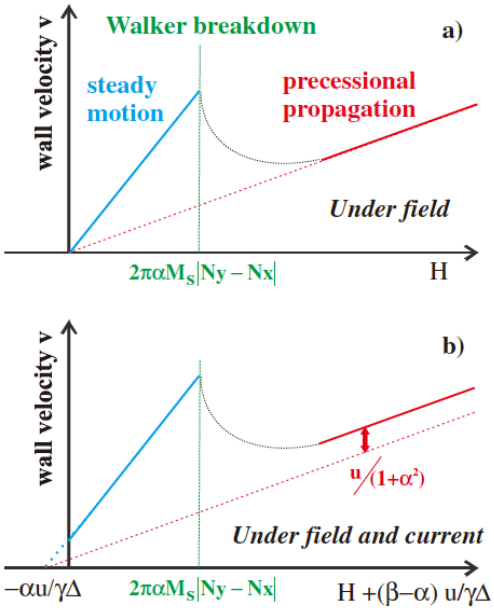
The averaged velocity of the domain wall motion decreases due to the change of the DW motion direction with time.

When Walker's breakdown occurs, the magnetisation rotates continuously and the direction of the magnetisation at the wall centre switches continuously.

The critical field for the Walker breakdown (Walker's field H_W) can be defined as

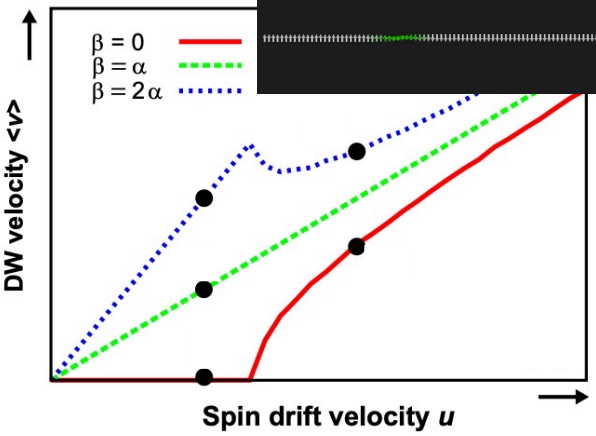
$$H_W = 2\pi M_S \alpha$$

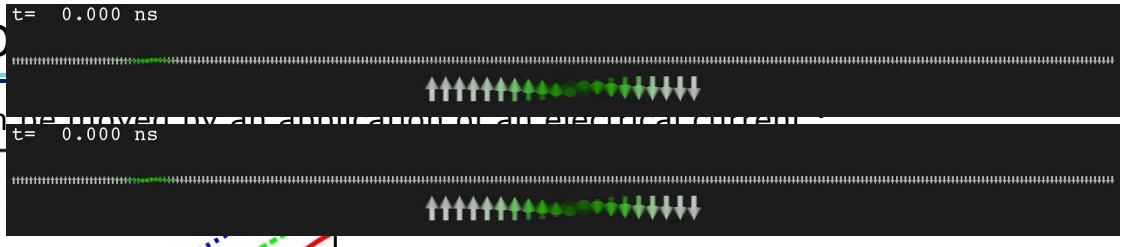
Here, M_s is the saturation magnetisation and α is the Gilbert damping constant.

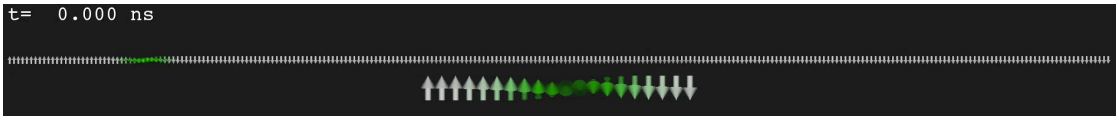


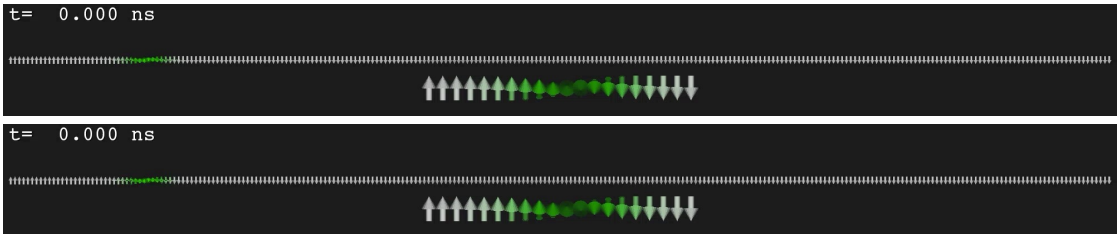
• N. L. Schryer and L. R. Walker *J. Appl. Phys.* **45**, 5406 (1974);
** A. Mougin *et al.*, *Euro. Phys. Lett.* **78**, 57007 (2007).

Domain wall can be moved by application of an electrical current :

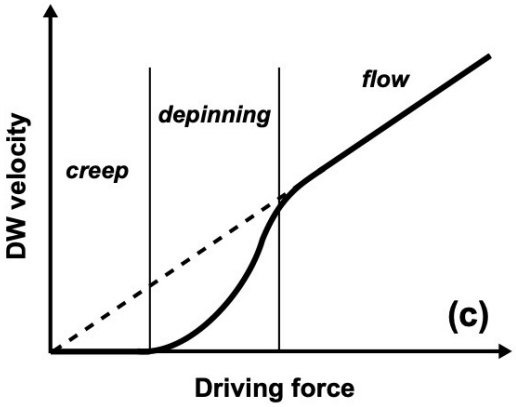








Domain wall can be moved by an application of either a magnetic field or an electrical current : *



By solving Landau-Lifschits-Gilbert- Slonczewski equation,

$$\frac{\partial \vec{M}}{\partial t} = -\gamma \vec{m} \times \overrightarrow{H_{\mathrm{eff}}} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \frac{\gamma}{d} \vec{m} \times \left(\vec{m} \times \Delta \vec{J_{\mathrm{S}}} \right)$$

where H_{eff} : an effective magnetic field, γ : the gyromagnetic ratio and α : the Gilbert damping constant.

$$|\gamma| = \frac{g \mu_{\mathrm{B}}}{h}$$

where g : Lange's g-factor, μ_{B} : the Bohr magneton and h : the Planck constant.

$$\alpha = \frac{|\gamma| \Delta H}{2\omega}$$

where ΔH : the full width half maximum of a ferromagnetic resonance and ω : the resonant frequency.

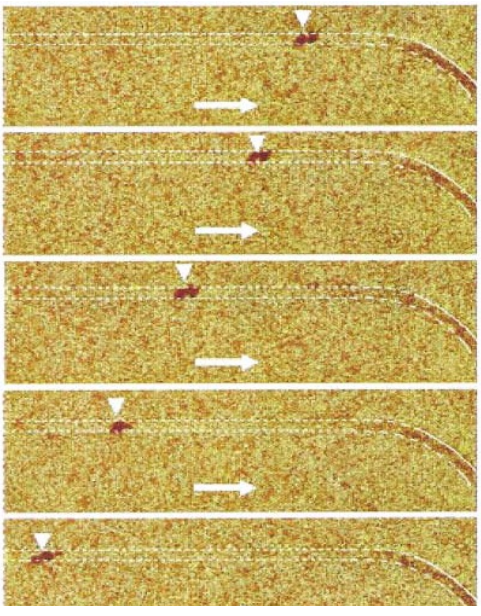
β is .

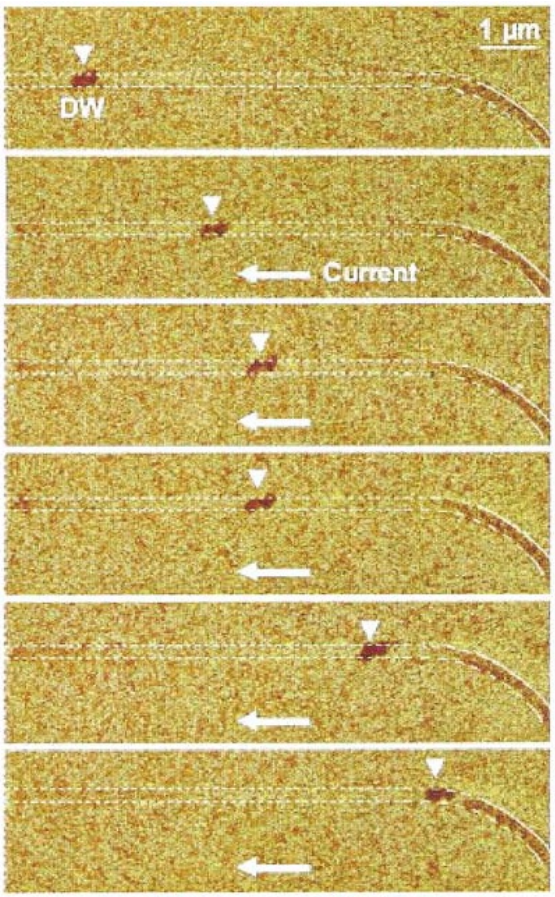
* A. Hirohata *et al.*, *J. Magn. Magn. Mater.* 509, 166711 (2020).

Domain Wall Displacement

For fast operation spin transfer torque (STT) will be used to move the walls.

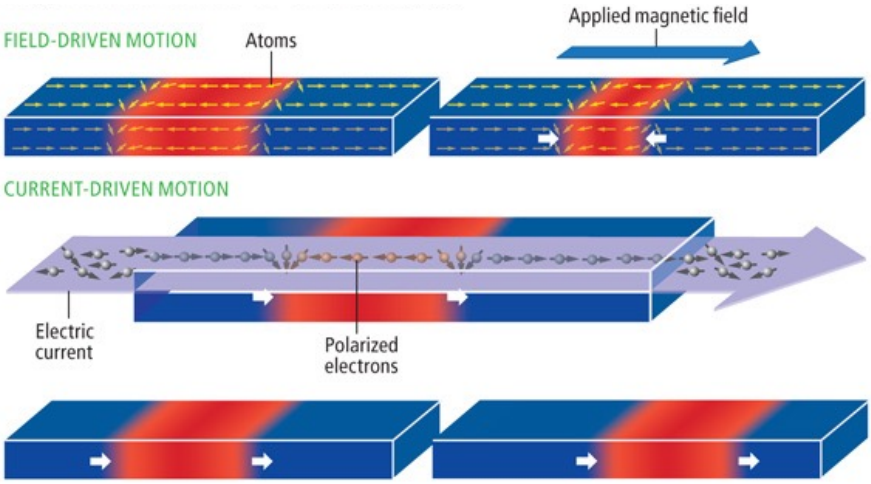
This requires a narrow track, possibly down to 100 nm, so that the STT dominates the Lorentz field.





In 2008, 3-bit racetrack memory was demonstrated by Stuart S. P. Parkin (IBM) : *

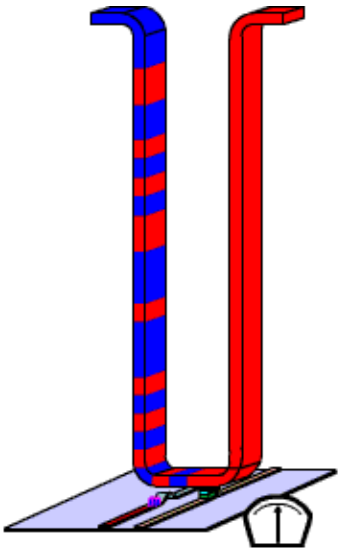
- Utilise domain-wall motion by STT



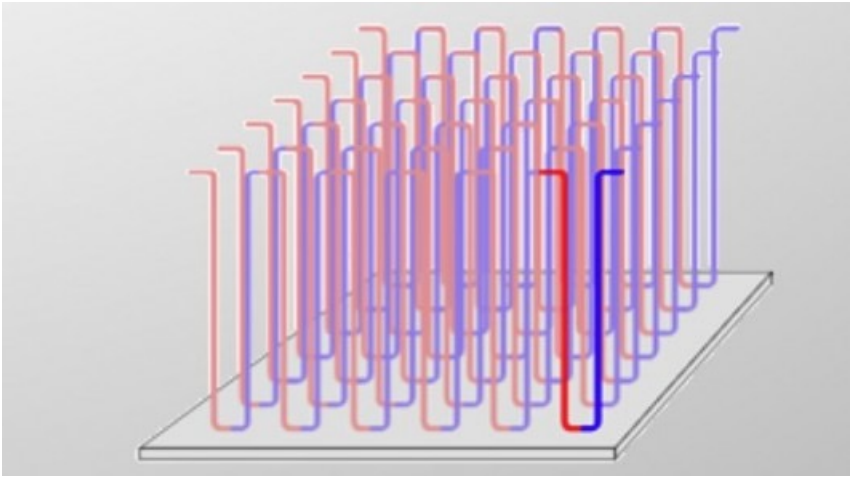
* http://www.i-micronews.com/news/IBM-moves-closer-class-memory,1231.html;
* S. S. P. Parkin, *Sci. Am.* 300, 76 (2009).

Racetrack-Memory Properties

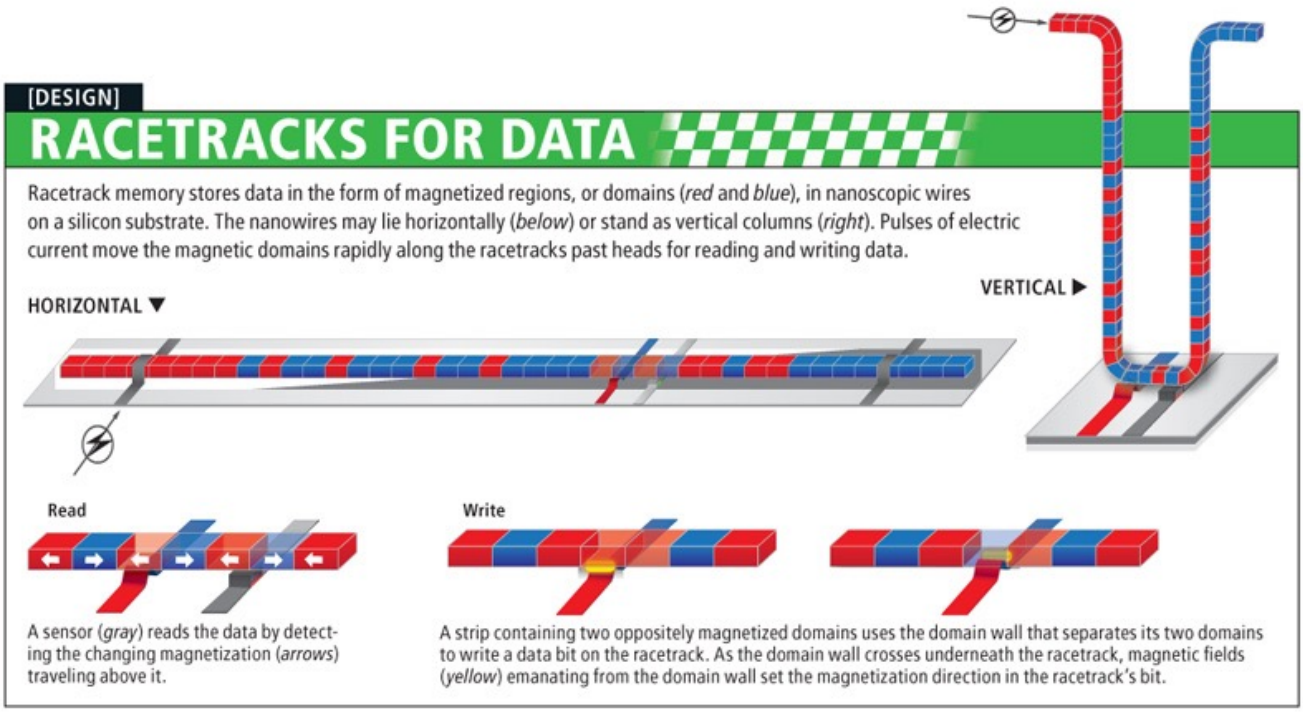
Racetrack memory architecture :



- ✓ Utilise magnetic domain walls
- ✓ "1" : head-to-head wall
- ✓ "0" : tail-to-tail wall
- ✓ CMOS process compatible
- ✓ 3-dimensional (3D) structure
- × Reproducible domain-wall trapping
- × 3D fabrication



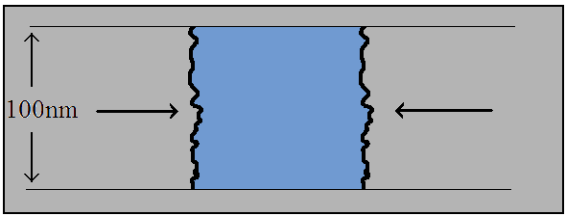
Fully electrical read-out / write-in :



* S. S. P. Parkin, *Sci. Am.* 300, 76 (2009).

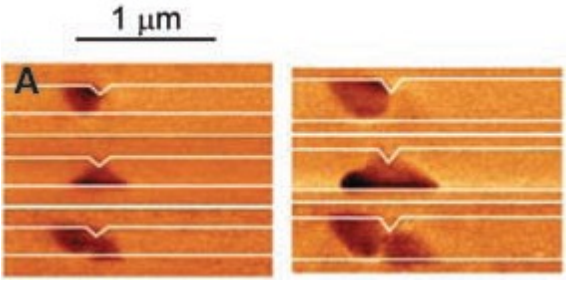
Basis of Racetrack Memory

Information can be stored in domains separated by head to head or tail to tail domain walls.



Typically 10 to 100 DWs can be contained in a 1 to 10 μm wire.

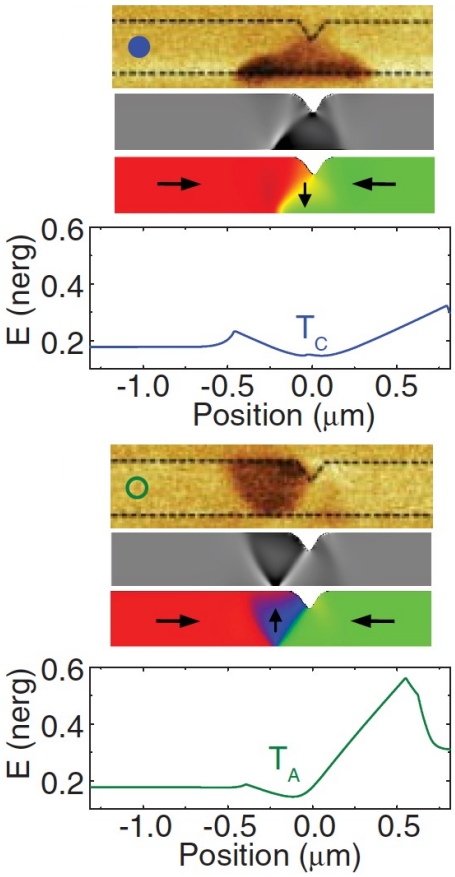
This is equivalent to Gbits/in^2 in a 2D array and can be extended to 3D.



For any DW memory it is required to have DW pins.

The separation between the DW pins determined the recording density.

The IBM system uses notches cut into the sides of the wire.



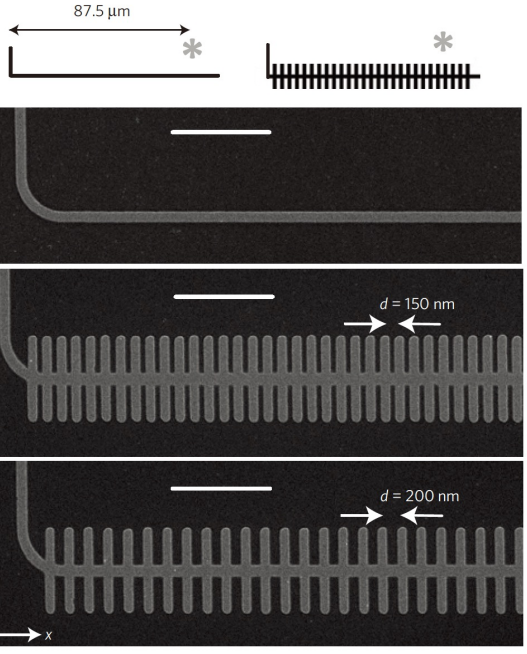
* M. Hayashi *et al.*, *Phys. Rev. Lett.* **97**, 207205 (2006).

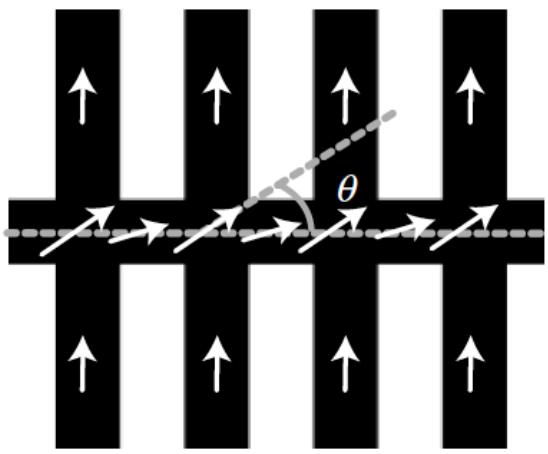
Domain Wall Pins - Combs

Lewis *et al.* use steps in the substrate.

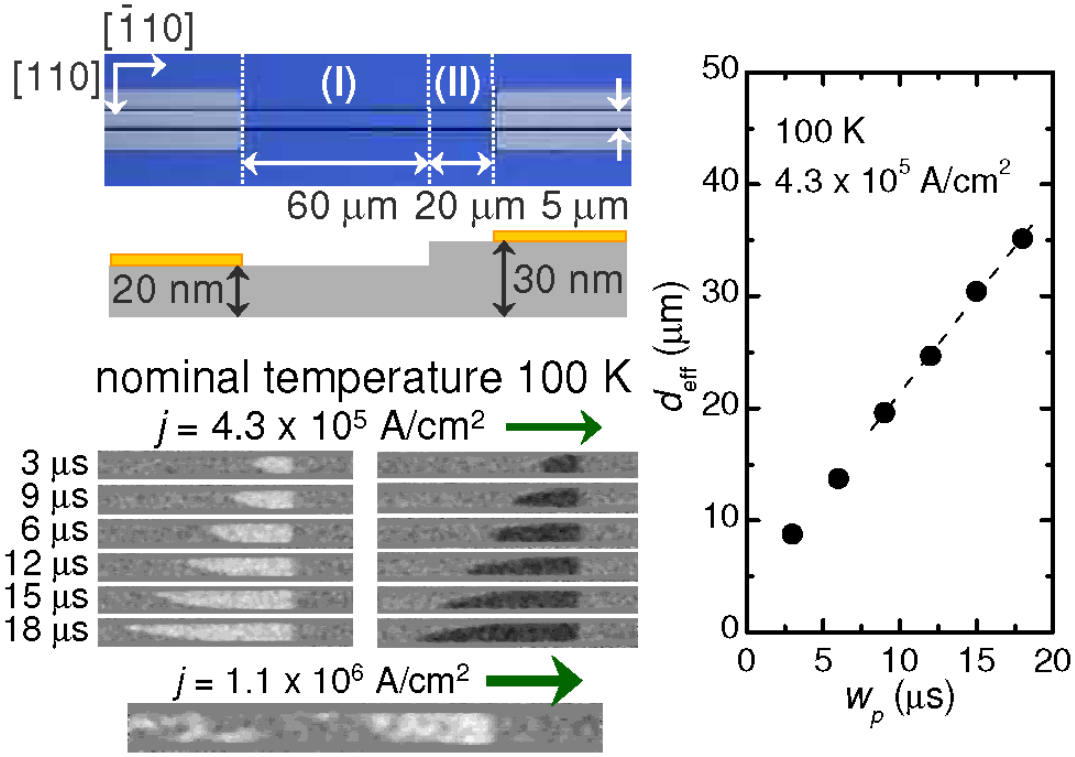
All these solutions are expensive.

Also these types of pin are not controllable and may not give uniform pinning strengths.





Yamanouchi *et al.* use steps in the substrate.



* M. Yamanouchi *et al.*, *Nature* **428**, 539 (2004).

Domain Wall Pins - Exchange Bias

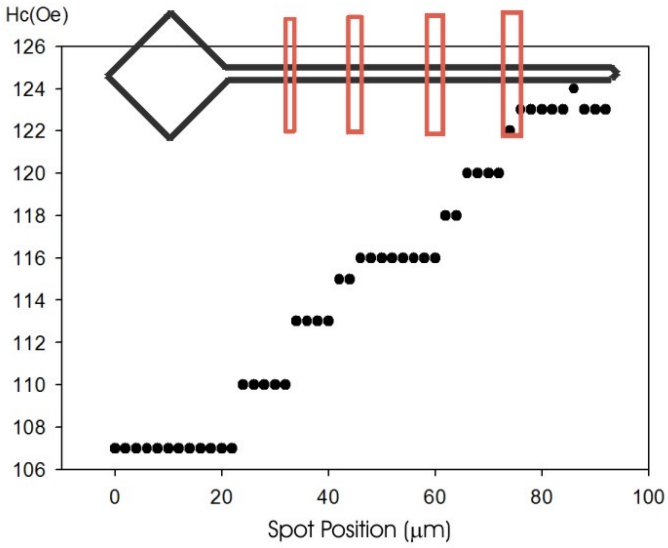
The strength of an exchange bias domain wall pin will depend on: *

- anisotropy of the material.
- size of the pin.
- thickness of the F wire.

Control of the anisotropy through EB has previously been shown. **

The size of the pin is the wire width.

We may also be able to compress the wall width using exchange bias.



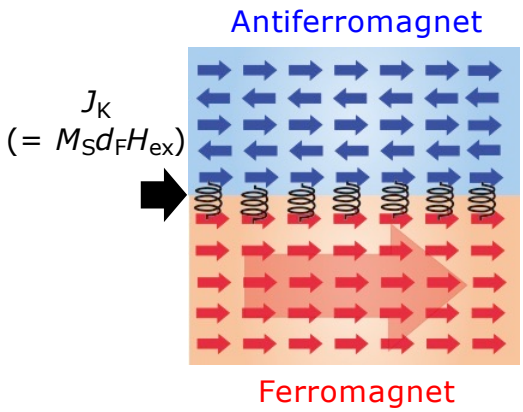
* K. O'Grady, A. Hirohata, G. Vallejo-Fernandez, *Exchange Bias Racetrack Memory*, UK Pat. 1218010.5 (2013);

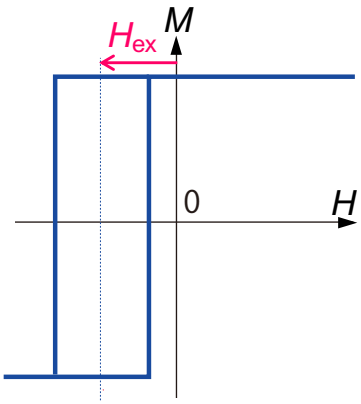
Exchange bias occurs when a ferromagnet (FM) is in intimate contact with an antiferromagnet (AF).

When field cooled nominally from near the Néel temperature (T_N) of the AF a loop shifted by H_{ex} results and the coercivity increases.

The materials used are typically IrMn/CoFe.

Despite being discovered in 1956, until recently we have had little understanding of this effect. *

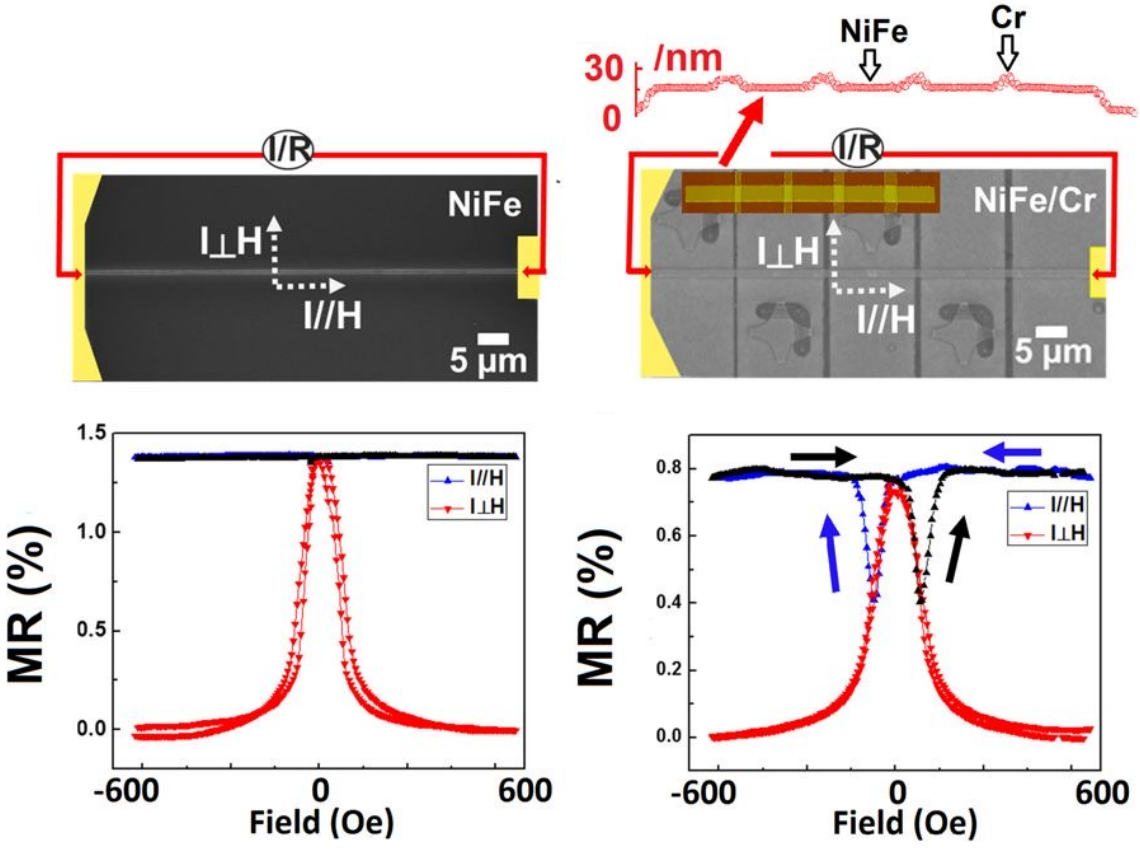




* K. O'Grady, L. E. Fernandez-Outon, G. Vallejo-Fernandez *J. Magn. Magn. Mater.* **322**, 883 (2010).
** I. Polenciuc *et al.*, *Appl. Phys. Lett.* **105**, 162406 (2014).

Domain Wall Pins – Metal Diffusion

Selective ion implantation can form a domain wall pin : *



Year Reported	Velocity(m/s)	Orientation	Material	J (A/cm^2)
2004		In plane	NiFe	~10^8
2008	Up to	In plane	NiFe	
2011	Up to	Perpendicular	Pt/Co	
2015	Up to 1000	Perpendicular	Co/Ni/Co/Ru/Co/Ni/Co	

The latest racetrack with 100 DWs would give 100 times higher density than MRAM.

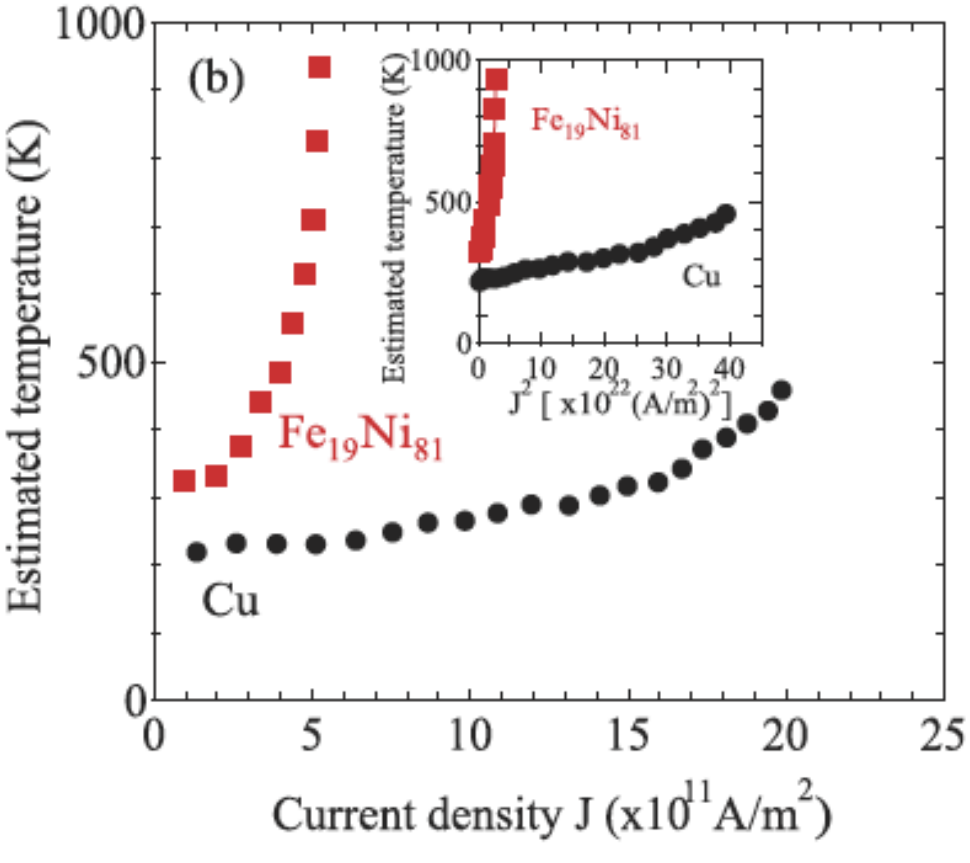
For a 100µm racetrack the read frequency would be of about 1GHz.

Racetrack technology is very flexible either giving high storage density, either giving very high access speeds.

Yamaguchi *et al.* Phys. Rev. Lett. **92**, 077205 (2004)
Parkin *et al*. Science 320, 190–194 (2008).
Miron *et al*. Nat Mat **12**, 299–303 (2013)
Ryu *et al.* Nature Commun. 5, 3910 (2014)
Parkin *et al.* Nature Nanotechnology **10**, 195–198 (2015)

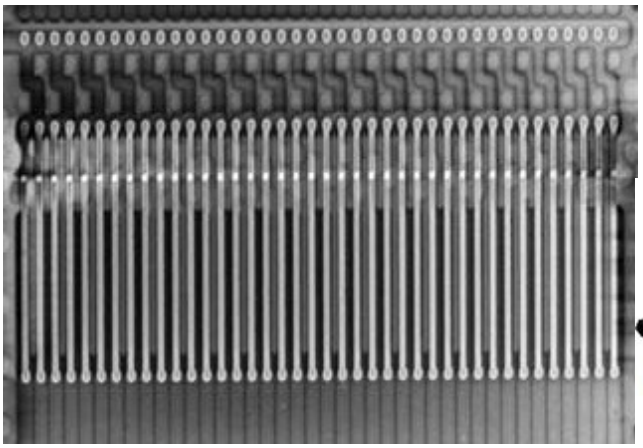
Joule Heating

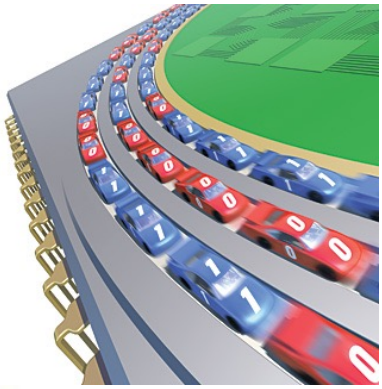
Current-introduction also generates Joule heating : *

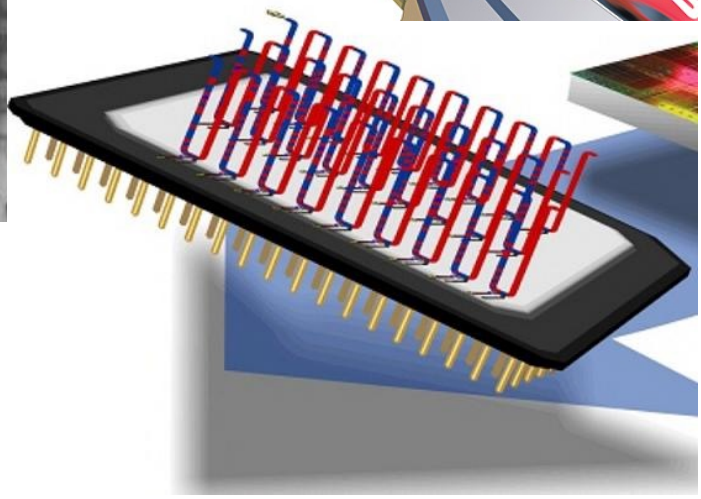


MRAM cell structure :

- 150 nm wide, 20 nm thick and 10 mm long ferromagnetic wires
- CMOS implementation







* http://www.ibm.com/

Information Technology Pyramid

Layered structures between CPU and storages : *