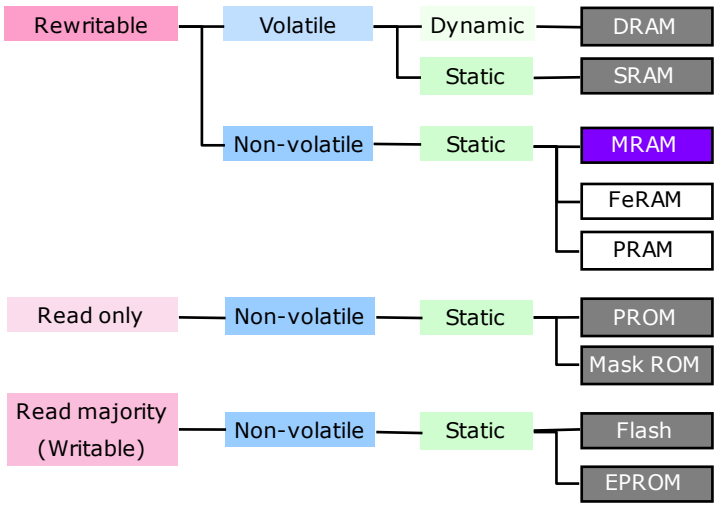
02 Magnetic Random Access Memory

- Non-volatility
- Read-out operation
- Spin-transfer torque
- Coherent tunnelling
- Perpendicular magnetisation
- Content addressable memory

10:00 11/February/2016 Thursday (B/B 103)

Memory Types



* http://www.semiconductorjapan.net/serial/lesson/12.html

Advantages of MRAM

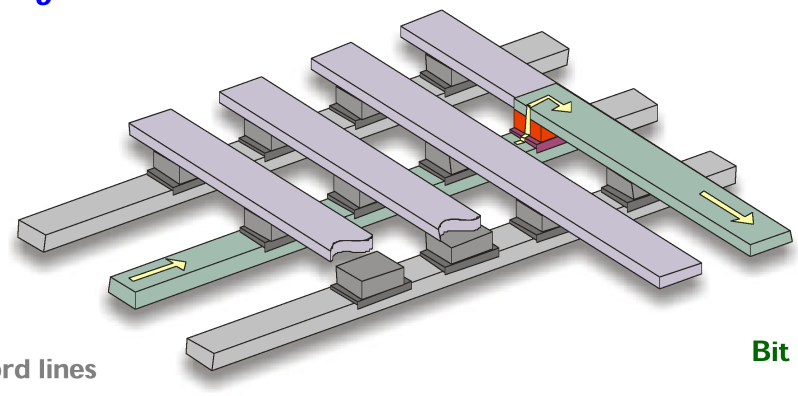
	MRAM	FeRAM	FLASH	DRAM	SRAM	1'' HDD
Non-volatality	✓	✓	✓	×	×	✓
Read time	300 ns (GMR) <60 ns (TMR)	100 ~ 200 ns	50 ns	✓	✓✓	~ 10 ms
Write time	< 10 ns	~100 ns	~ 10 μs	✓	✓✓	~ 10 ms
Repetition	> 10^{15}	10^{9} ~ 10^{12}	10^{5}	✓	✓✓	✓✓
Cell density	6 ~ 12 F^2	8 F^2	4 F^2	✓	△	—
Chip capacity	> 1 Gb	< 10 Mb	> 1 Gb			—
Power	< 10 mW	> 10 mW	△	△	✓	> 1 W
Soft error hardness	✓	✓	✓	✓	×	✓
Process cost	RT process	HT process	Lower bit cost			Lowest bit cost

* *After* K. Inomata, *J. Magn. Soc. Jpn.* 23, 1826 (1999).

Magnetic Random Access Memory

Basic operation of magnetic random access memory (MRAM) :

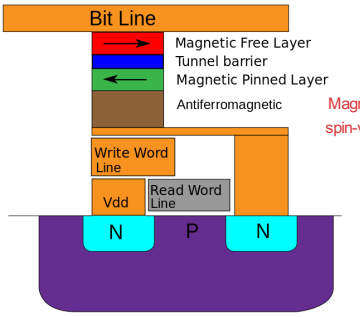
Reading



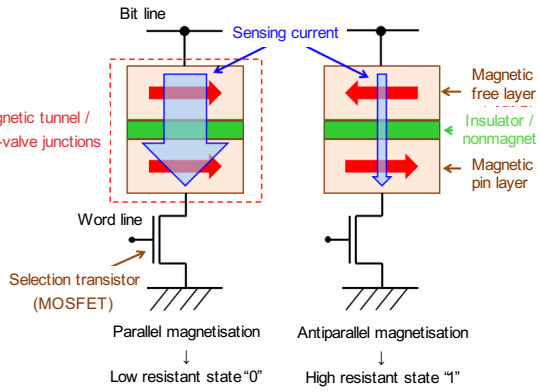
* S. S. P. Parkin, *1st Int'l Sch. on Spintronics and Quantum Info. Tech.*, May 13-15, 201 (Maui, HI, USA).

MRAM Cell

MRAM cell structure :



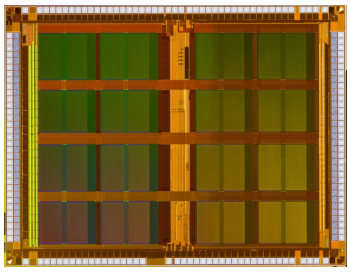
MRAM read-out :

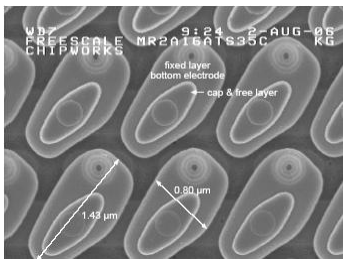


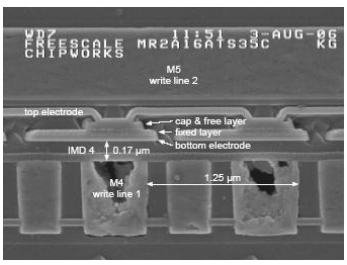
* http://www.wikipedia.org/

MRAM Products

Freescale (now EverSpin Technologies) 4 Mbit MRAM :



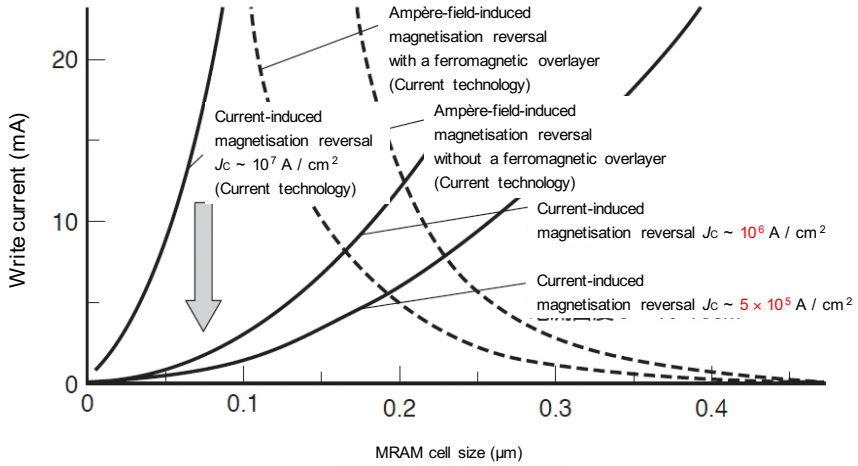




* http://www.freescale.com/;
** http://www.chipworks.com/blogs.aspx?id=2514

Improved MRAM Operation

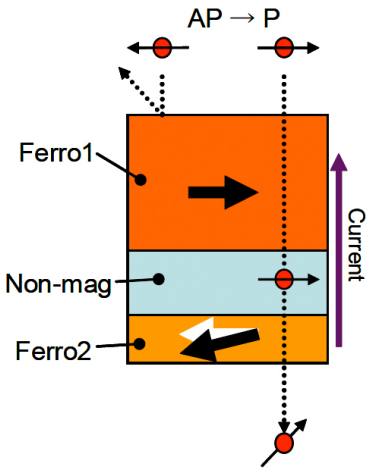
Required writing currents for several techniques dependent upon cell size :



* S. Nakamura, Y. Saito and H. Morise, *Toshiba Rev.* 61, 40 (2006).

Current-Induced Magnetisation Reversal

Anti-parallel (AP) ↔ parallel (P) reversal in a GMR / TMR junction :

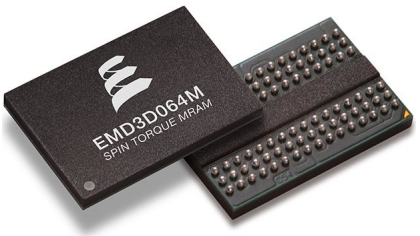


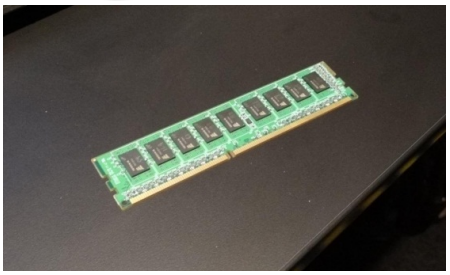
Spin-transfer torque (STT) **

* M. Oogane and T. Miyazaki, "Magnetic Random Access Memory," in *Epitaxial Ferromagnetic Films and Spintronic Applications*, A. Hirohata and Y. Otani (Eds.) (Research Signpost, Kerala, 2009) p. 335.
** J. Slonczewski, *J. Magn. Magn. Mater.* 159, L1 (1996); L. Berger, *Phys. Rev. B* 54, 9353 (1996).

STT-MRAM Products

In 2012, EverSpin Technologies introduced 64 Mbit MRAM :





500x Performance…

	NAND	MRAM
Density	64Gb	1Gb
Power	80mW	400mW
4kB Write IOPS	800	400k
Cost/GB	1	50

…at only 5x Power

* http://www.everspin.com/

STT-MRAM Advantages 1

ST-MRAM *Delivering 10x better Price/Performance*

Cloud Storage Needs:

- More content & users, instant access
- Better response times from storage
- Predictable balanced performance

Nanosecond-class MRAM Storage

NAND SSD

500x Performance…

	NAND	MRAM
Density	64Gb	1Gb
Latency	50us	45ns
4kB Write IOPS	800	400k
Cost/GB	1	50

…at only 50x Cost/GB

MRAM SSD

EVERSPIN TECHNOLOGIES The MRAM Company

13

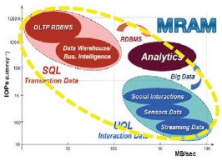
* http://www.everspin.com/

STT-MRAM Advantages 2

ST-MRAM *Delivering 100x Power/Performance*

Data Center needs:

- Number of servers & CPU cores exploding
- Better bandwidth & IOPS to handle Big Data
- More performance @ less power to scale up



High Performance, Power-Efficient MRAM Storage

NAND SSD

500x Performance…

	NAND	MRAM
Density	64Gb	1Gb
Power	80mW	400mW
4kB Write IOPS	800	400k
Cost/GB	1	50

…at only 5x Power

MRAM SSD

EVERSPIN TECHNOLOGIES The MRAM Company

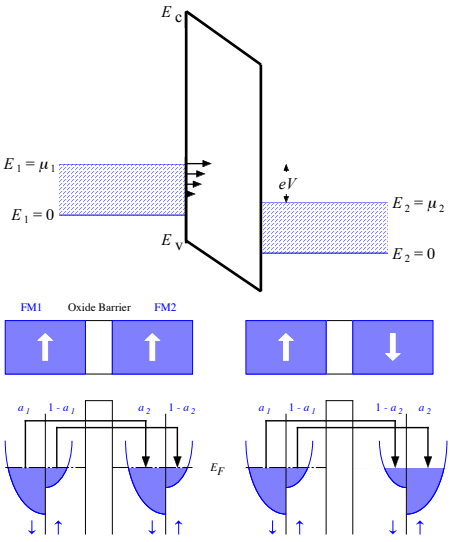
14

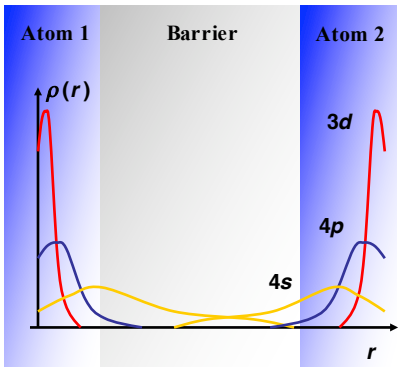
* http://www.everspin.com/

Spin-Dependent Electron Tunneling

Jullière's model :

FM / insulator / FM junctions *

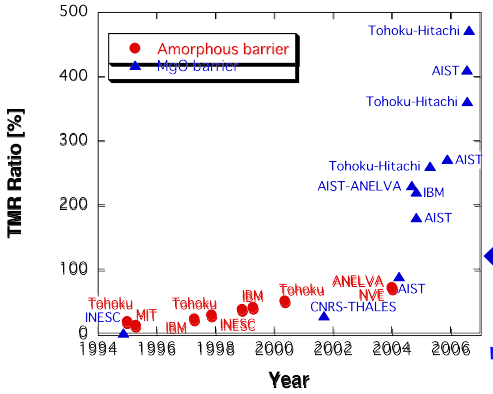




* M. Jullière., *Phys. Rep.* 54A, 225 (1975).

TMR for Device Applications

Recent progress in TMR ratios :



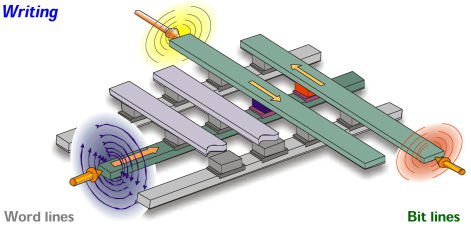
> 400 % (604 % in 2008) TMR ratio has been achieved !

↓

> Gbit MRAM can be realised.

NOT following Jullière's model : **

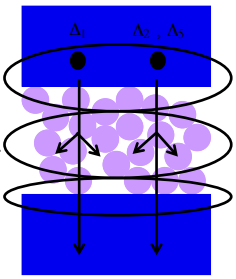
$$TMR = 2P_1P_2 / (1 - P_1P_2)$$



* M. Jullière., *Phys. Rep.* 54A, 225 (1975);
** S. S. P. Parkin, *1st Int'l Sch. on Spintronics and Quantum Info. Tech.*, May 13-15, 2001 (Maui, HI, USA).

Improved Tunnel Barriers

Conventional amorphous barriers : *

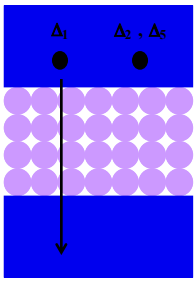


Defects in the barrier

Disorder at the interface :
- FM over-oxidation
- lattice defects

Disorder at the interface :
- FM over-oxidation
- lattice defects
- island growth of the barrier

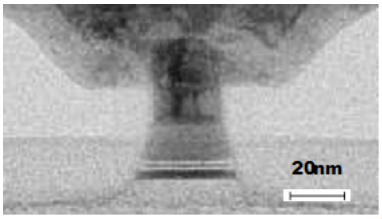
Epitaxial (oriented) barriers : *

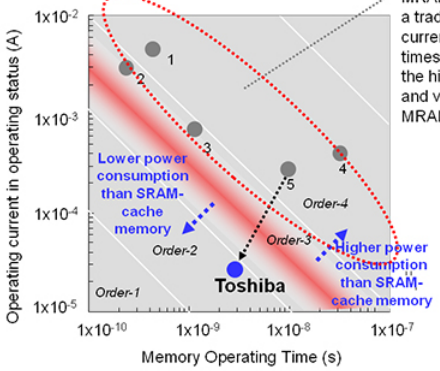


* *After* S. Yuasa *et al.*, *28th Annual Conference on Magnetics*, Sep. 21-24, 2004 (Okinawa, Japan).

Perpendicular MTJ

In 2007, Toshiba demonstrated STT operation with perpendicular magnetisation : *





Typical operating range of STT-MRAM or MRAM. There has been a trade-off between operating current and memory operating times: the faster the performance the higher the power consumption and vice-versa. Toshiba's STT-MRAM overcomes this.

Breakthrough!

Power consumption is about one-tenth that of prior prototypes.

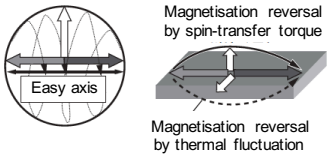
Reported devices

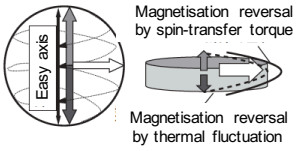
1 Spintech APL 2009
2 Univ. of Minnesota J. Phys. D 2012
3 IBM APL 2011
4 Spintech APL 2011
5 Toshiba IEDM 2008

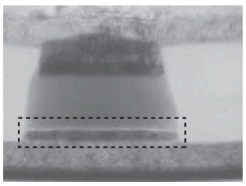
* http://www.toshiba.co.jp/

Advantages of Perpendicular MTJ

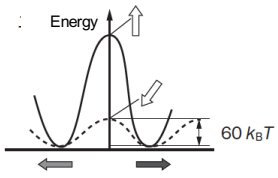
Energy barrier can be lowered using perpendicular magnetisation : *

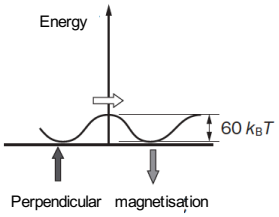


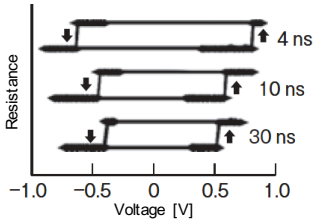




50-nm perpendicular MTJ





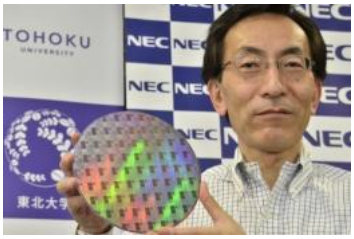


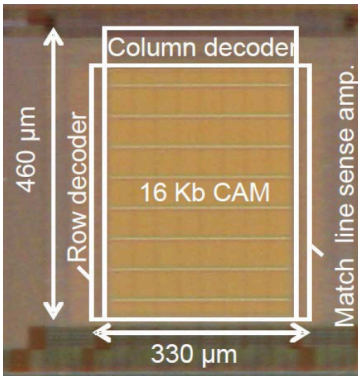
* http://www.toshiba.co.jp/

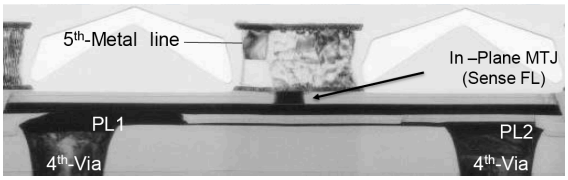
Content Addressable Memory (CAM)

In 2011, NEC and Tohoku University announced a new memory concept : *

- ✓Fast latency : 5 ns
- ✓Low power consumption : 9.4 mW
- ✓50 % area reduction by sharing transistors





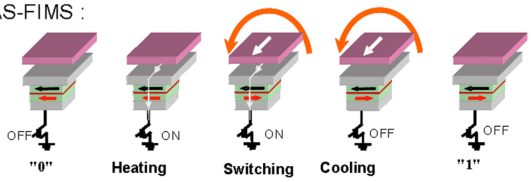


* http://www.csis.tohoku.ac.jp/

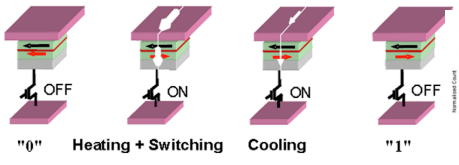
Thermally Assisted (TA)-MRAM

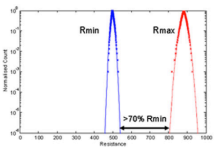
Crocus demonstrated 1-Mbit MRAM with thermally assisted STT operation : *

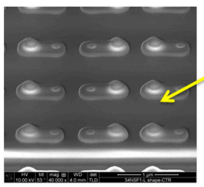
TAS-FIMS :

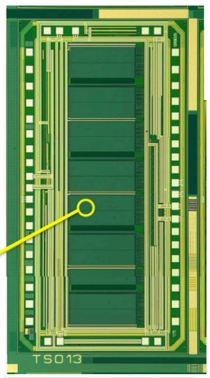


TAS-STT :





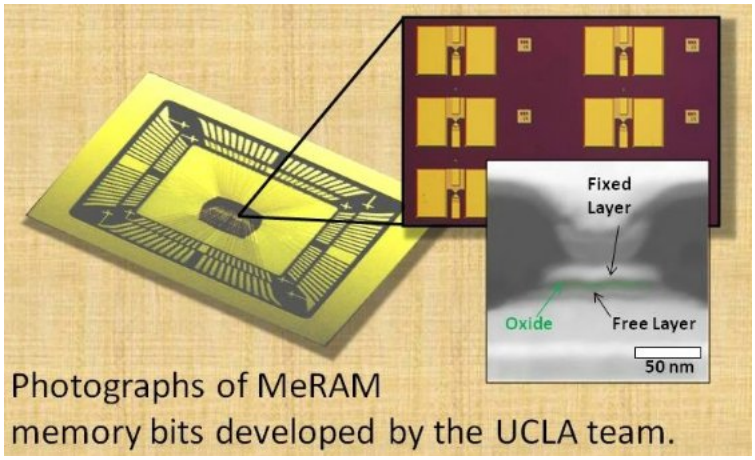




* I. L. Prejbeanu *et al.*, *J. Phys. D: Appl. Phys.* **46**, 074002 (2013).

Reduced Energy Consumption

3-orders of reduction in energy consumption was demonstrated by UCLA team : *



Voltage-induced magnetisation reversal was used.

* http://newsroom.ucla.edu/portal/ucla/ucla-engineers-have-developed-241538.aspx

Comparison between Next-Generation Memories

Table 1 Representative NV-RAM Available 2007-08 Comparison of large-capacity NV-RAM chips available on the merchandise market.

Memory type		FeRAM (ferroelectric memory)		MRAM (magnetic memory)	PRAM (phase-change memory)	
Manufacturer		Fujitsu	Ramtron International	Freescale Semiconductor	Intel	Samsung Electronics
Model		MB85R2001/ MB85R2002	FM22L16	MR2A16A	Not disclosed	Not disclosed
Capacity		2-Mbit	4-Mbit	4-Mbit	128-Mbit/1-Gbit/2-Gbit	512-Mbit*1
Word configuration		256Kwords x 8/128Kwords x 16	256Kwords x 16	256Kwords x 16	Not disclosed	32Mword x 16*1
Access time		100ns	55ns	35ns	Read equivalent to DRAM, NOR Flash memory, etc	Not disclosed
Cycle time		150ns	110ns	35ns	Read time tens of ns to 100ns, equivalent to DRAM, NOR Flash memory, etc. Write expected to be significantly faster than NOR Flash memory, but slightly longer than DRAM.*2	Write about 1/30th of NOR Flash memory*2
Operating current consumption	Read	15mA	18mA	80mA	Not disclosed	Not disclosed
	Write	15mA	18mA	155mA	Not disclosed	Not disclosed
Standby current		50μA	150μA	12mA	Not disclosed	Not disclosed
Rewrites		10^{10} or higher	10^{14} times or higher	Effectively infinite (more than 10^{16} times)	10^6 times or higher	10^5 times or higher*1
Supply voltage		3V to 3.6V	2.7V to 3.6V	3V to 3.6V	3V /3V /1.8V	1.8V*1
Operating temperature		-20°C to +85°C	-40°C to +85°C	0 to +70°C (general use), -40°C to +85°C (industrial use), -40°C to +105°C (expanded temp range)	Not disclosed	Not disclosed
Data retention time		10 years min (+55°C)	10 years	20 years	10 years min (+85°C)	10 years min (+85°C)*1
Interface		Pseudo-SRAM compliant with asynchronous SRAM	Asynchronous SRAM	Asynchronous SRAM	Not disclosed	Not disclosed
Package		48-pin TSOP	44-pin TSOP	44-pin TSOP	Not disclosed	Not disclosed
Manufacturing technology		180nm	130nm	Not disclosed	90nm/45nm/45nm	90nm*1
Memory cell configuration		1 transistor + 1 capacitor	1 transistor + 1 capacitor (stacked)	1 transistor + 1 TMR device	Not disclosed	1 diode + 1 phase-change device
Memory cell area		Not disclosed	0.71μm²	Not disclosed	Not disclosed	0.0467μm²
Sample shipment start		Samples shipping	Samples shipping	Samples shipping	3Q 2007 / Not disclosed / Not disclosed	2008
Volume production start		Volume production stance established	Small-lot production from 3Q 2007, volume production from 4Q 2007	General-application chips in volume production now	Early 2008 /2H or later 2008 /2H 2008	Not disclosed
Chip manufacturing		In-house	Outsourced to Texas Instruments	In-house	In-house	In-house
Price		Samples ¥2000	US$19.00 in lots of 10,000	US$14.99 in lots of 10,000 for general use, US$24.99 in lots of 10,000 for expanded temp range	Not disclosed	Not disclosed

*1 Specifications for Samsung Electronics products have not been disclosed. Specifications shown are those announced at IEDM 2006 by Samsung Electronics in December 2006 for a 512-Mbit prototype.
*2 Most NOR Flash memory has a write time (per-byte) of about 6μs to 7μs.

* http://techon.nikkeibp.co.jp/article/HONSHI/20070926/139715/