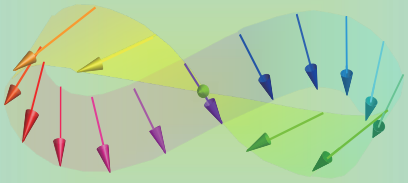
Nanoelectronics
01



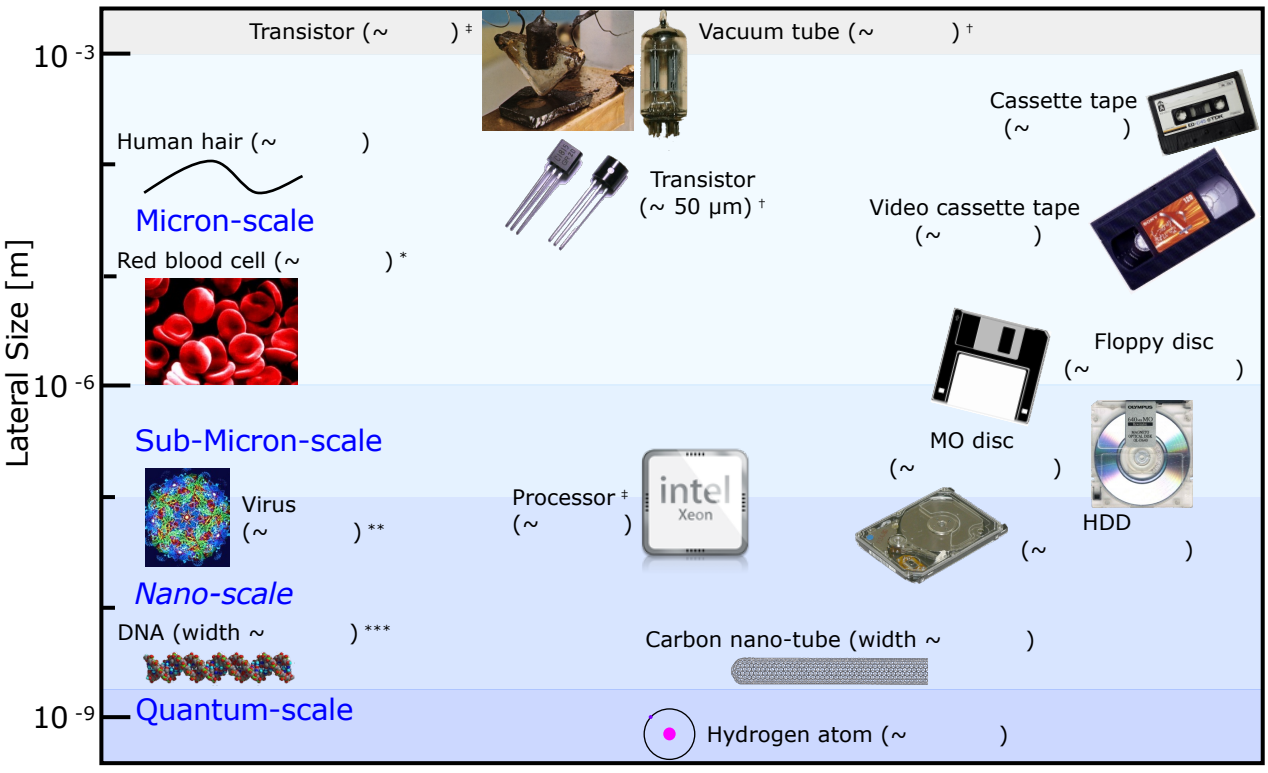
Atsufumi Hirohata

Department of Electronic Engineering

THE UNIVERSITY of York

09:00 Thursday, 19/January/2023 (ENV 005)

Go into Nano-Scale



* http://www.esa.int/esaKIDSen/SEMOC68LURE_LifeinSpace_1.html

** http://www.guardian.co.uk/pictures/image/0,8543,-11404142447,00.html

*** http://www.wired.com/medtech/health/news/2003/02/57674

† http://www.wikipedia.org/

‡ S. M. Sze, *Physics of Semiconductor Devices* (John Wiley, New York, 1981).

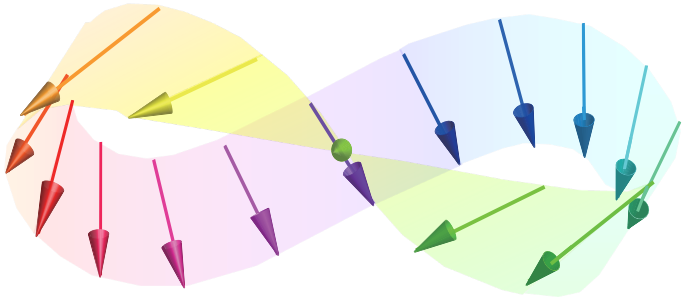
Nanoelectronics

Electronics

- Electron transport
- Magnetism

Material Sciences

- Semiconductors
- Ferromagnets
- Superconductors
- Organic materials



Physics

- Electromagnetism
- Quantum mechanics

Contents of Nanoelectronics

Lectures : Atsufumi Hirohata (atsufumi.hirohata@york.ac.uk, P/Z 019)

Electrical transport in nanometric scale (Weeks 2 ~ 10)

All lectures will be uploaded weekly in advance at

http://www-users.york.ac.uk/~ah566/lectures/lectures.html & Wiki

09:00 ~ 10:00 Mons. (P/T 005A)

12:00 ~ 13:00 Weds. (P/T 005A)

I. Introduction to nanoelectronics (01)

II. Electromagnetism (02 & 03)

III. Basics of quantum mechanics (04 ~ 06)

IV. Application of quantum mechanics (07, 10, 11, 13 & 14)

V. Nanodevices (08, 09, 12, 15 ~ 18)

Workshops : (1/2 towards the final mark)

Equation solving in quantum physics (Weeks 2, 4, 6 & 8)

All workshop questions will be uploaded weekly in advance at

http://www-users.york.ac.uk/~ah566/lectures/lectures.html & VLE

15:00 ~ 16:00 Fris. (LFA 204X)

Submit your answers via VLE by 12:00 on Thus. On Weeks 4, 6, 8 & 9.

Examination : (1/2 towards the final mark)

Online exam (Equation solving + Essay)

References

General textbooks in nanoelectronics :

K. Goser, P. Glosekotter and J. Diestuhl, *Nanoelectronics and Nanosystems* (Springer, Berlin, 2004); which covers all the topics in the field.

V. V. Mitin, V. A. Kochelap and M. A. Stroscio, *Introduction to Nanoelectronics* (Cambridge University Press, Cambridge, 2008); which focuses on semiconductor nanoelectronics and nanodevices.

Douglas Natelson, *Nanostructures and Nanotechnology* (Cambridge University Press, Cambridge, 2016); which focueses on nanoelectronic devices.

General textbooks in quantum mechanics :

D. J. Griffiths, *Introduction to Quantum Mechanics* (Cambridge University Press, Cambridge, 2017); which covers all the topics in the field.

G. L. Squires, *Problems in Quantum Mechanics* (Cambridge University Press, Cambridge, 1995); which provides broad problems with solutions.

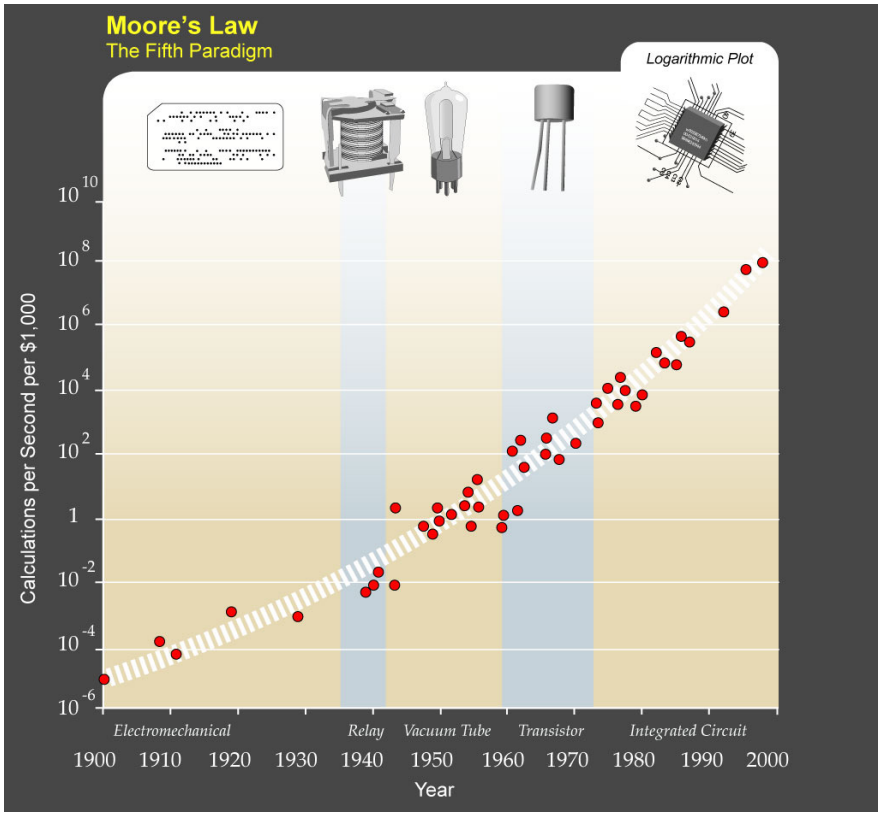
A. Berera and L. Del Debbio, *Quantum Mechanics* (Cambridge University Press, Cambridge, 2022); which provides selected problems with solutions.

Lecture notes / slides : http://www-users.york.ac.uk/~ah566/lectures/lectures.html
& Wiki

01 Micro- to *Nano-Electronics* ?

- Device miniaturisation
- Micron / nanometre
- Nanofabrication
- New functionality
- Electron transport

Miniaturisation of Data Processors



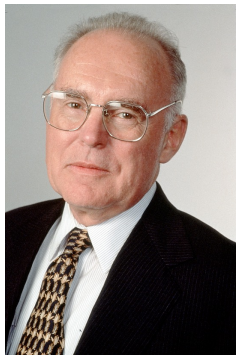
* http://www.wikipedia.org/

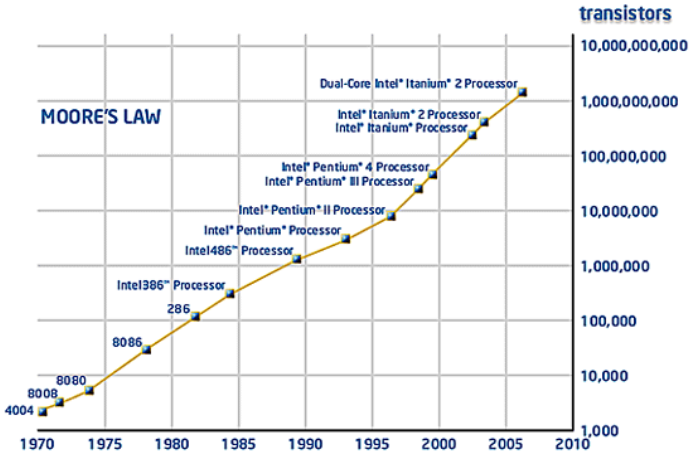
Miniaturisation and Integration in Semiconductor Devices

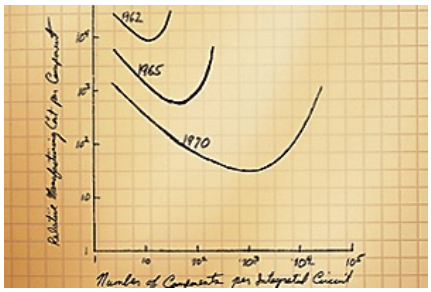
Moore's law :

"The number of transistors on a chip will double every months." (1965)

10 years later he revised this to "every months."





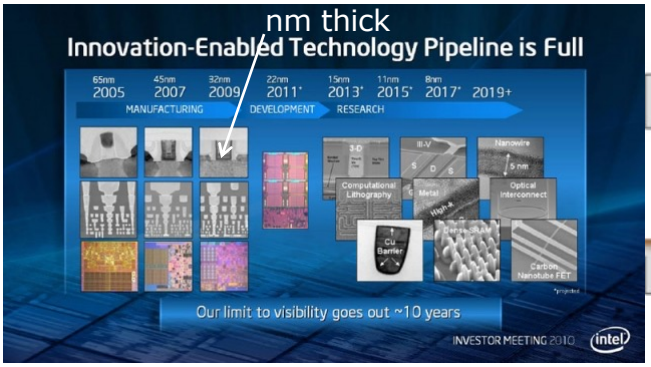


→ The development speed becomes even faster !

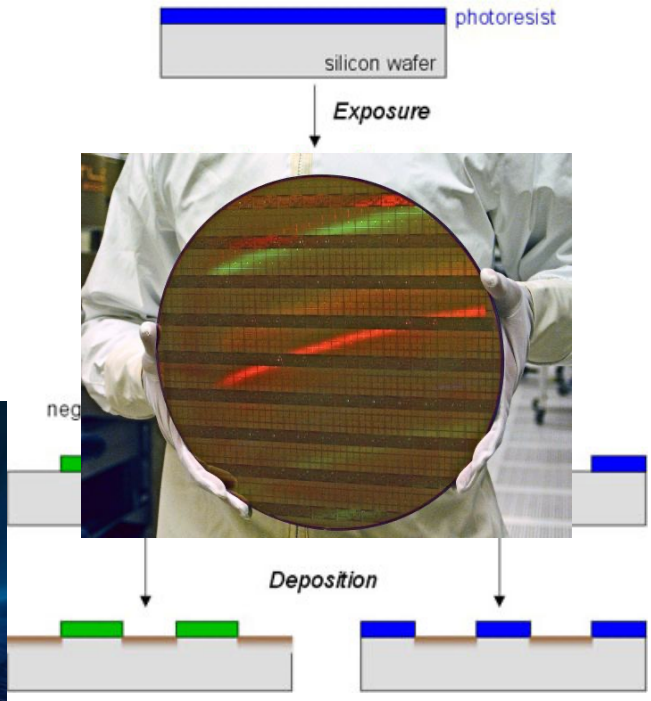
* http://www.intel.com/

Current Semiconductor Technology

45-nm rule :



Nanofabrication method :



* http://www.intel.com/
** http://www.kodak.com/

Roadmap for Si-Based Devices

Table 1.1 A roadmap for Si-based microelectronics (predictions of the Semiconductor Industry Association)

	1995	1998	2001	2004	2007	2010
Memories, DRAM						
Bits per chip	64 M	256 M	1 G	4 G	16 G	64 G
Cost per bit (milli-cent)	0.017	0.007	0.003	0.001	0.0005	0.0002
Cost per chip (US$)	11	18	30	40	80	130
Logic, microprocessors						
Transistors per cm^2	4 M	7 M	13 M	25 M	50 M	90 M
Cost per transistor (milli-cent)	1	0.5	0.2	0.1	0.05	0.02
Power supply (V)	3.3	2.5	1.8	1.5	1.2	0.9
Parameters						
Minimum feature size (μm)	0.35	0.25	0.18	0.13	0.10	0.07
Wafer size (in.)	8	8	12	12	16	16
Electrical defect density per m^2	240	160	140	120	100	25

The data are from U. König, *Physica Scripta*, **T68**, 90, 1996.

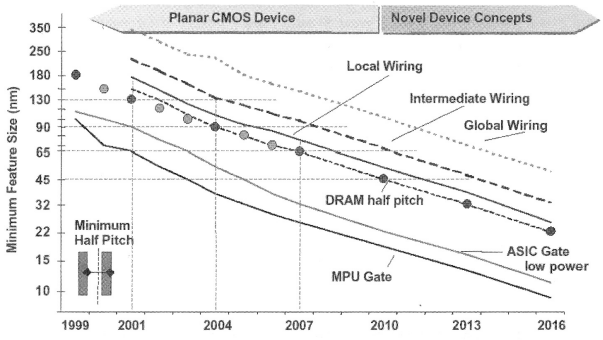
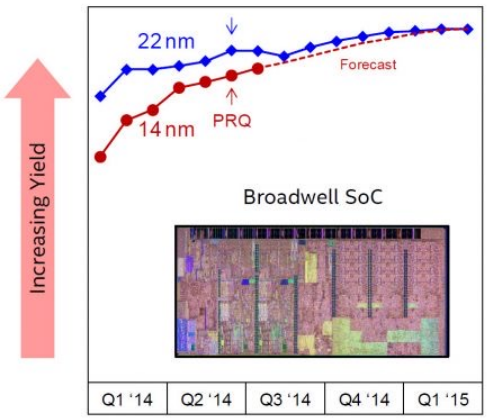


Figure 1.1 Technology nodes and minimum feature sizes from application ITRS Roadmap: MPU, Micro Processing Unit; ASIC, Application-Specific Integrated Circuit. Used with permission, from W. Klingenstein (2002). *Technology Roadmap for Semiconductors.* http://broadband02.ici.ro/program/klingenstein_3d.pdf, page 15. © InfineonTechnologies AG, 2002.

* V. V. Mitin, V. A. Kochelap and M. A. Stroscio, *Introduction to Nanoelectronics* (Cambridge University Press, Cambridge, 2008).

14 nm Broadwell SoC Yield Trend



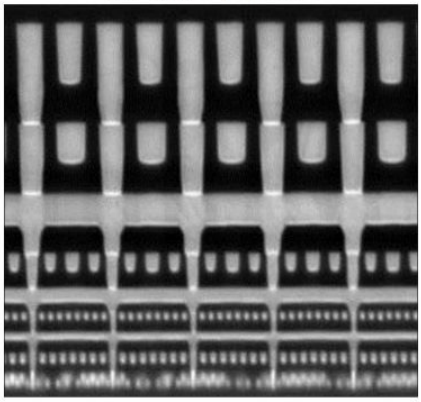
22 nm data are shifted to align date of lead product qual
Depicts relative health, lines not to scale

- 14 nm product yield is now in healthy range with further improvements coming
- Process and lead product are qualified and in volume production
- 14 nm manufacturing fabs are located in Oregon (2014), Arizona (2014) and Ireland (2015)
- Production yield and wafer volume are projected to meet the needs of multiple 14 nm product ramps in 1H '15

Leadership Technologies are Never Easy (at First!)

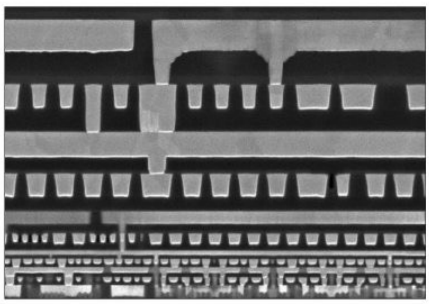
Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process

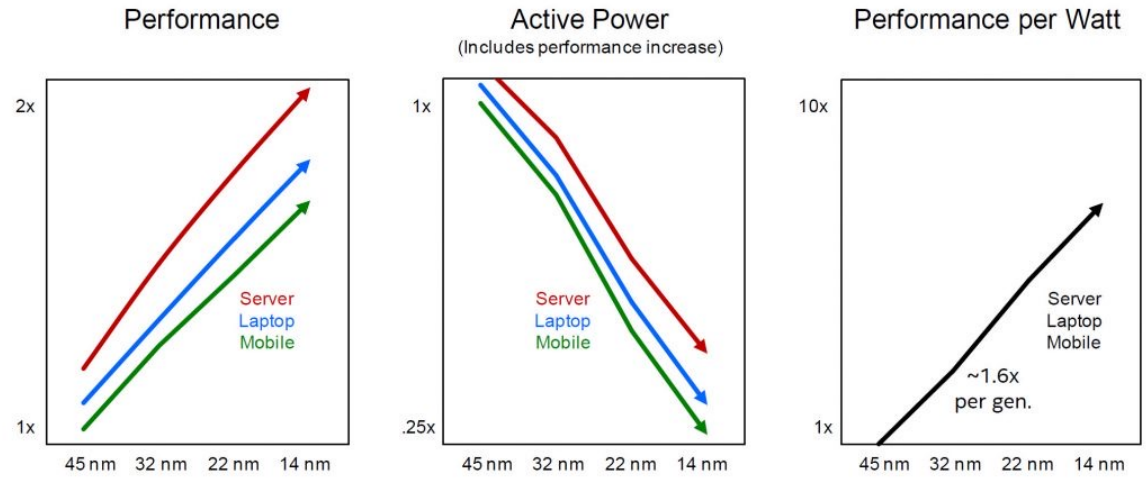


52 nm (0.65x) minimum pitch

52 nm Interconnect Pitch Provides Better-than-normal Interconnect Scaling

Advantages of Latest Chips

Product Benefits

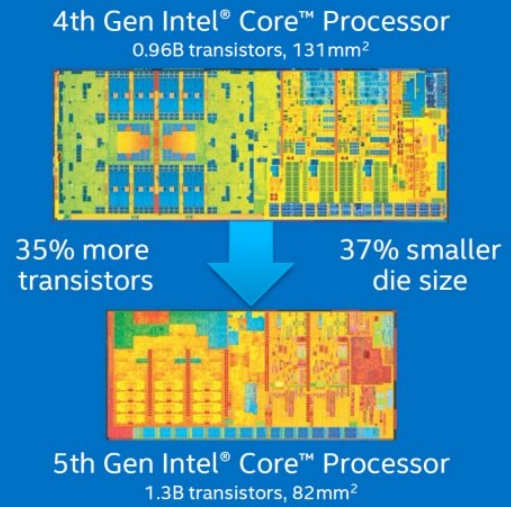


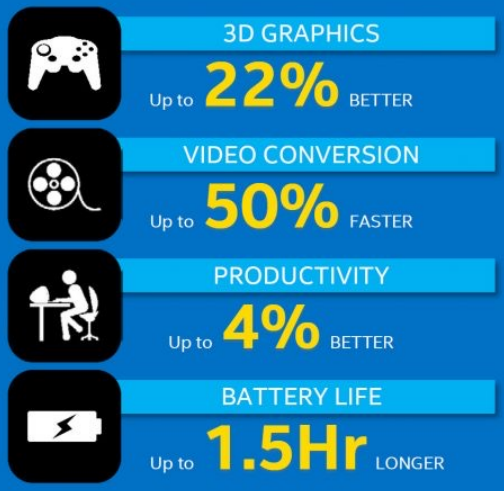
New technology generations provide improved performance and/or reduced power, but the key benefit is improved performance per watt

Improvements by Latest Chips

5th Gen Intel Core Processor Generational Improvements

Intel® Core™ i7-5600U Processor with Intel® HD Graphics 5500 compared to 4th Generation Intel® Core™ i7-4600U with Intel® HD Graphics 4400[1]





Source: Intel. Productivity: SYSmark 2014. 3D Graphics: 3DMark® IceStorm Unlimited v 1.2. Video Conversion: CyberLink® MediaEspresso® 6.5 video editing. Battery life: based on 40Whr battery capacity. Intel 1080p movie. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance

[1]Configuration detail in Appendix A

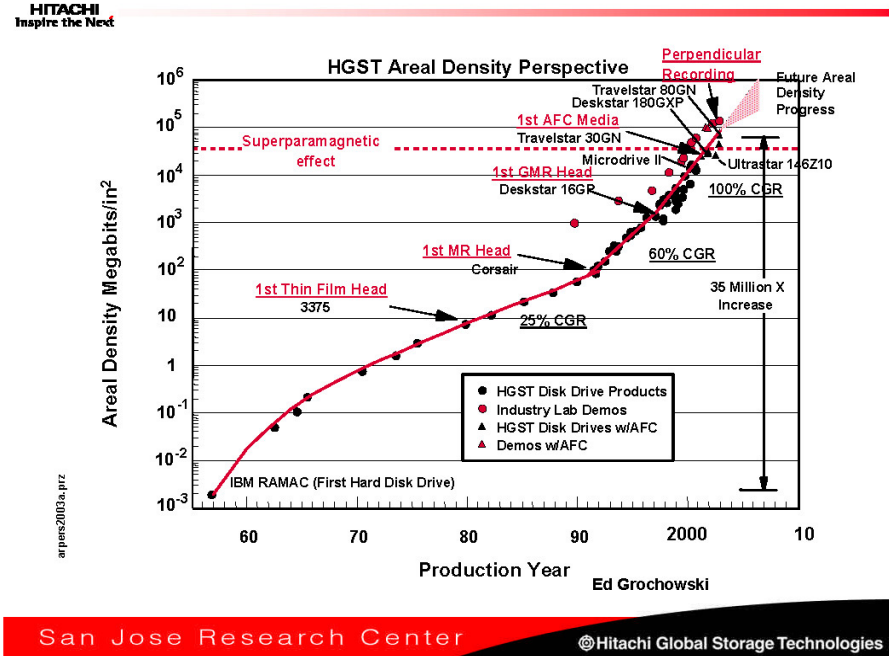
Increase in Recording Density of Hard Disc Drives

Similar to Moore's law :

Areal density in a hard disc drive (HDD) will double every months. (~ 1992)

After giant magnetoresistance (GMR) implementation,

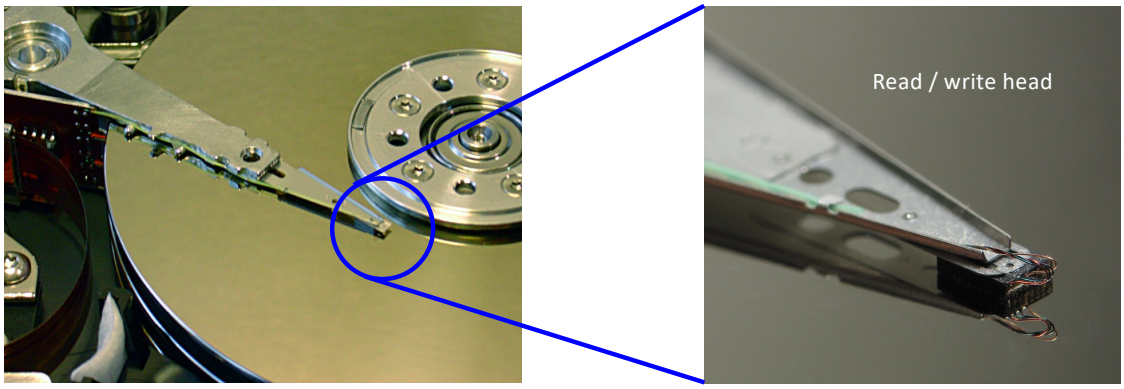
it will double less than every months. (1992 ~)



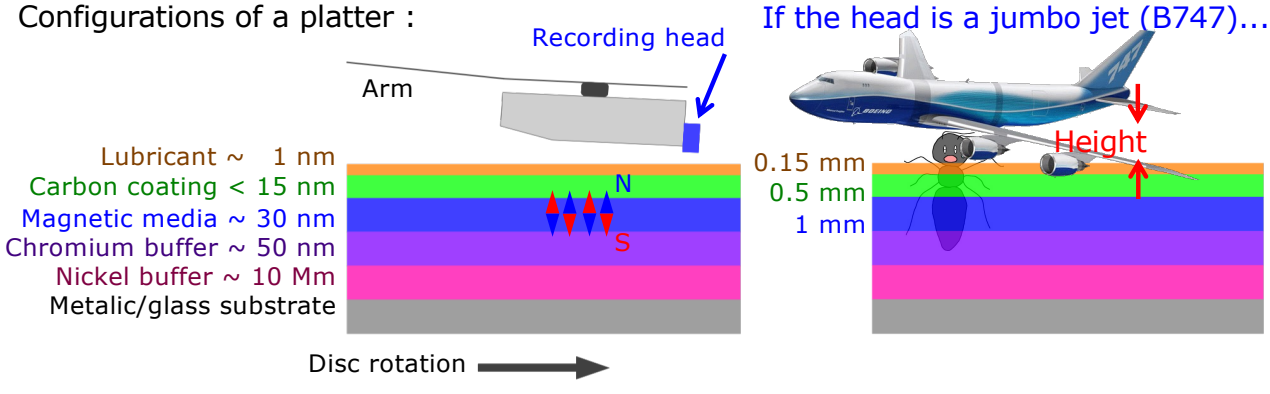
How Does a Recording Head Look Like ?

Recording media …

Recording head …



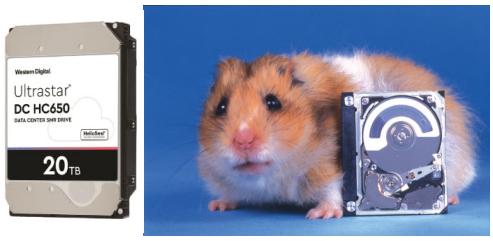
Configurations of a platter :



If the head is a jumbo jet (B747)...

Development of HDD

Recording density increases at ~ 100% / year :



First HDD in the world :

RAMMAC 305 (1956, IBM)

cm (in) platter × 50 = 4.4 MB

Mbit / in^2 920 kg

$ / GB

Current HDD :

Ultrastar DC HC650 (2020, WD)

cm (in) platter × 9 = 20 TB

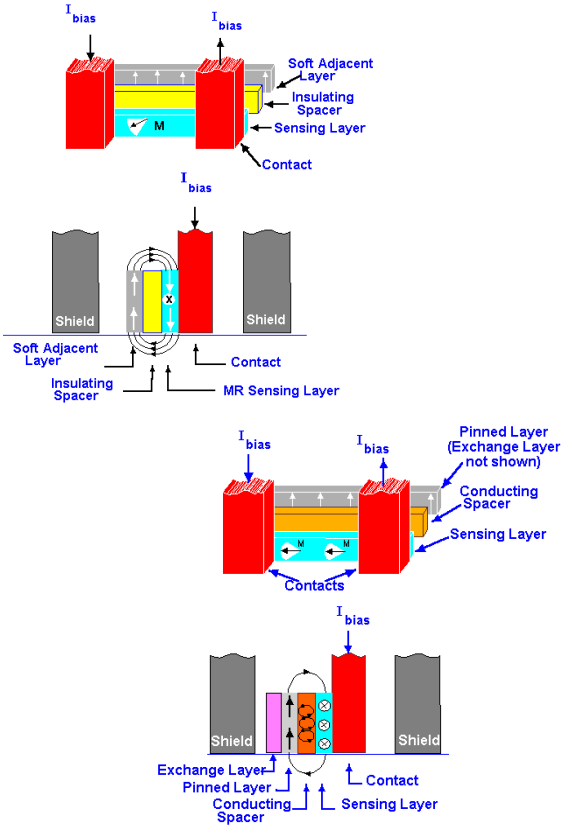
Tbit / in^2 690 g

$ 0.03 / GB

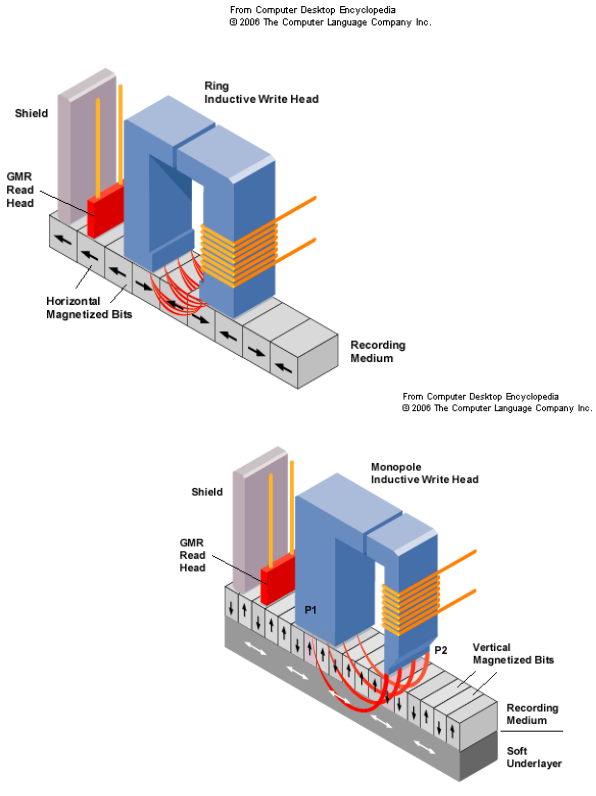
What can you get from such development ?

Current Magnetic Recording Technology

Anisotropic to Giant magnetoresistance :



Longitudinal to perpendicular recording :



* http://www.hitachigst.com/

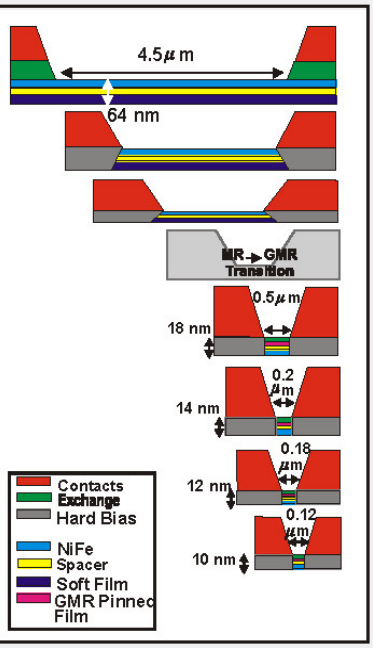
Miniaturisation in Magnetic Recording Technology

Size evolution of a recording head in a HDD :

HITACHI
Inspire the Next

MR/GMR Read Head Evolution

Year	Areal Density (gbits/in2)	Product
1991	0.132	Corsair
1992	0.260	Allicat
1993	0.354	Spitfire
1994	0.578	Ultrastar XP
1995	0.829	Ultrastar 2XP
	0.923	Travelstar 2LP
1996	1.32	Travelstar 2XP
	1.45	Travelstar VP
1997	2.64	Travelstar 5GS
	2.68	Deskstar 16GP
	3.12	Travelstar 6GN
1998	3.74	Travelstar 6GT
	4.1	Deskstar 25GP
	5.7	Travelstar 6GN
1999	5.3	Deskstar 37GP
	10.1	Travelstar 18GT
2000	7.04	Ultrastar 36LZX
	14.5	Deskstar 40GV
	17.1	Travelstar 30GT
2001	13.2	Ultrastar 73LZX
	25.7	Travelstarr 30GN
	29.7	Deskstar 120GXP
	34.0	Travelstar 40GN
2002	26.3	Ultrastar 146Z10
	45.5	Deskstar 180GXP
	29.7	Deskstar 120GXP
2003	70.0	Travelstar 80GN
2004	>100	
2005	>200	



Super2003a.prz

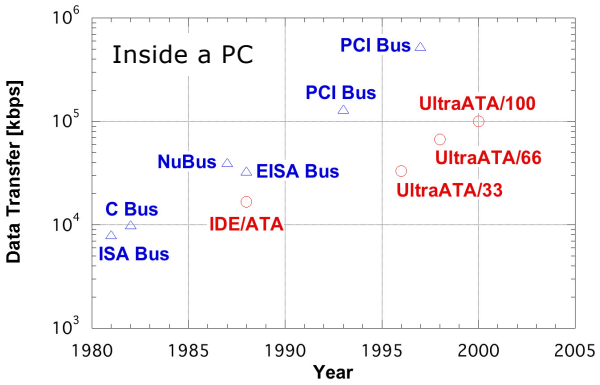
Ed Grochowski

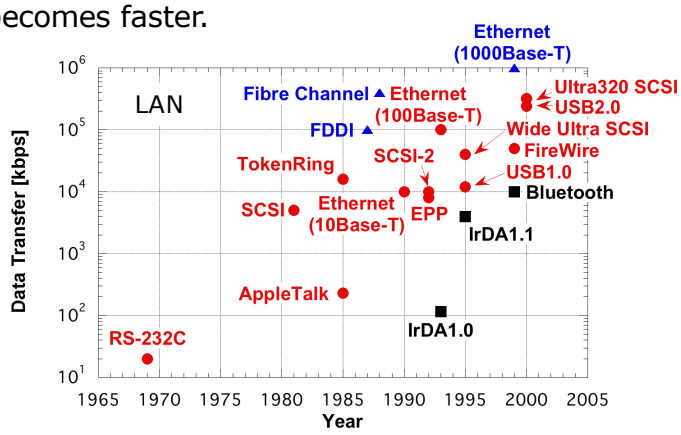
San Jose Research Center

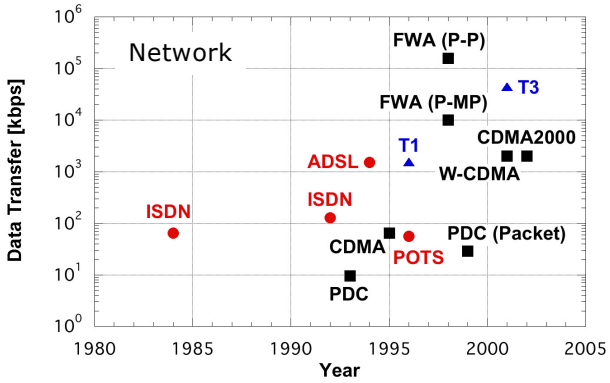
Hitachi Global Storage Technologies

Advancement in Communication Technologies

Similar to Moore's law : Data transfer becomes faster.







Advantages of Nano-Scale Miniaturisation

From microelectronics to nanoelectronics :

✓ Reduction of effective electron paths
✓ Reduction of electron scattering

→ Faster operation

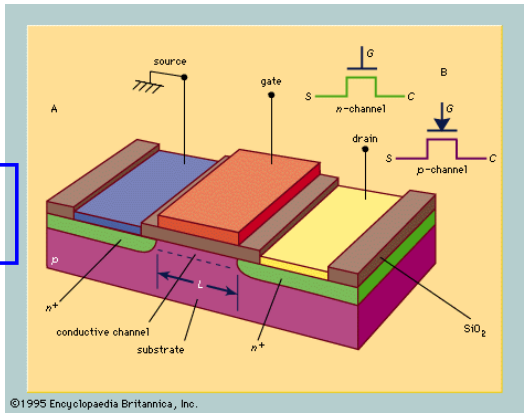
✗ More complicated fabrication processes
✗ Higher fabrication cost
✗ Larger distributions in device properties

✗ Leakage currents (insulator < 1nm thick)
✗ No electron confinement (path < 10 nm thick)

✗ Joule heating

→ Need to be solved in *Nanoelectronics*

- *Electromagnetism*
- *Quantum physics*
- *Nano-device fabrication*

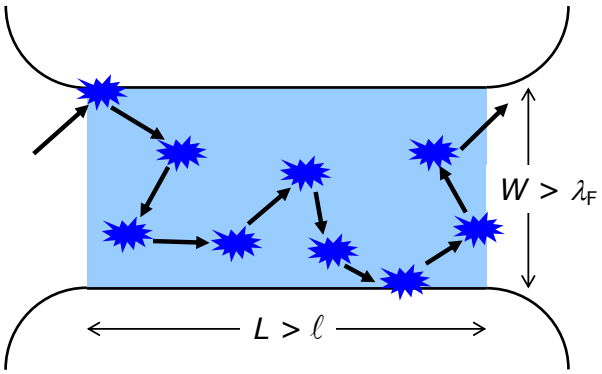


Electron Transport in a Nano-Device

transport :

Electron scattering

→ Electrical resistivity

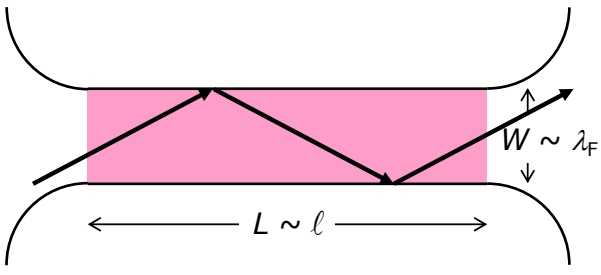


transport :

Negligible electron scattering

→ Negligible electrical resistivity

≈ Transport in a vacuum

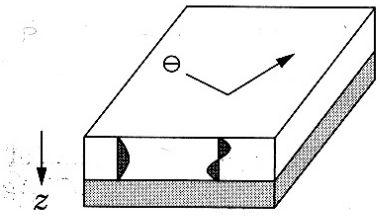


ℓ : electron mean free path (~ nm for Cu @ RT)

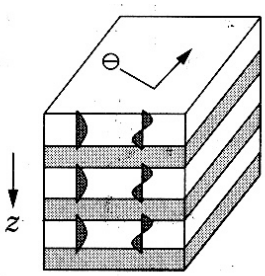
λ_F : Fermi wave length (~ nm)

Hot-electron

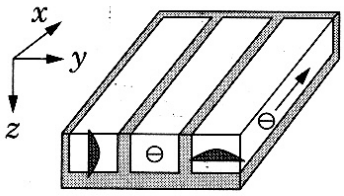
4 fundamental nano-device structures :



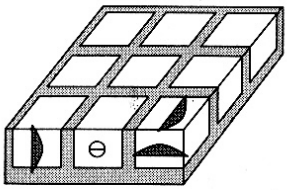
Ultrathin film (quantum well)



Superlattice (multilayer)



Quantum wire (nano-wire)



Quantum dot (nano-dot)

* H. Sakaki and N. Yokoyama, *Nanoelectronics* (Ohm-sha, Tokyo, 2004).