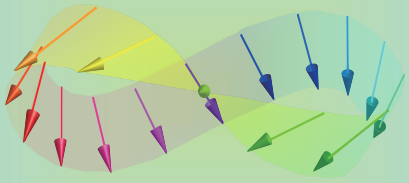
Nanoelectronics
08



Atsufumi Hirohata

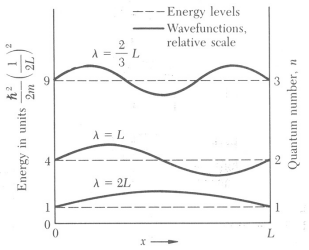
Department of Electronic Engineering

THE UNIVERSITY of York

12:00 Thursday, 09/February/2023 (P/T 005A)

Quick Review over the Last Lecture

1D quantum well :

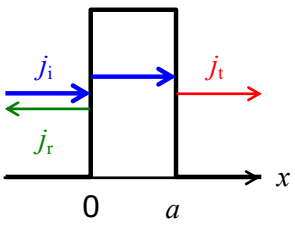


$$E = \frac{\hbar^2}{2m_0 a^2}\xi^2$$

→ ( )

Quantum tunnelling :

( ) + ( ) = 1

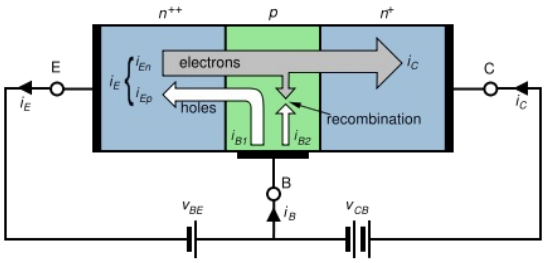


08 Tunnelling Nanodevices

- Esaki diode
- Resonant tunnelling
- Coulomb blockade
- Single electron transistor

Invention of a Transistor

First bipolar transistor (transfer resistor) was invented
by John Bardeen, William B. Schockley and Walter H. Brattain in 1947 :

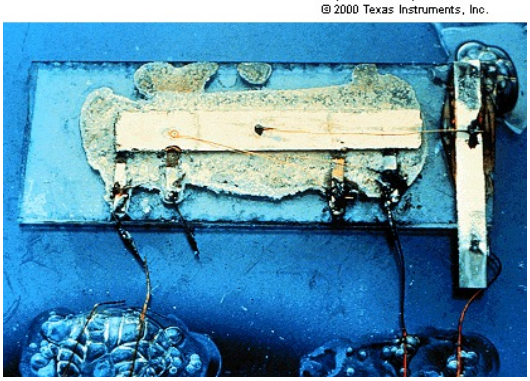


* http://www.wikipedia.org/; http://photos.aip.org/;
** S. M. Sze, *Physics of Semiconductor Devices* (John Wiley, New York, 1981).

Commercialisation and Integration of Transistors

In 1954, Texas Instruments commercialised the first Si transistor :

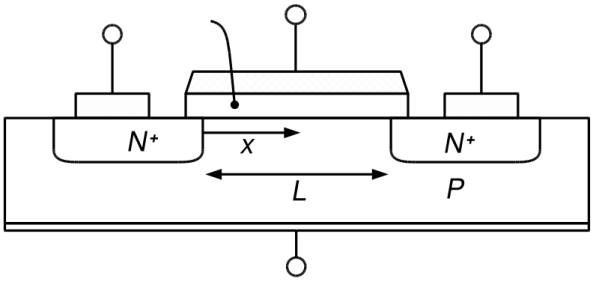
In 1958, Texas Instruments built the first integrated circuit on a Ge bar :

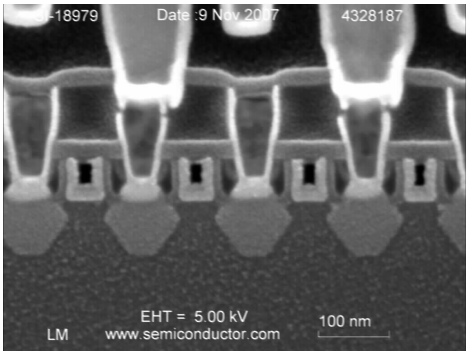


* http://computer.yourdictionary.com/

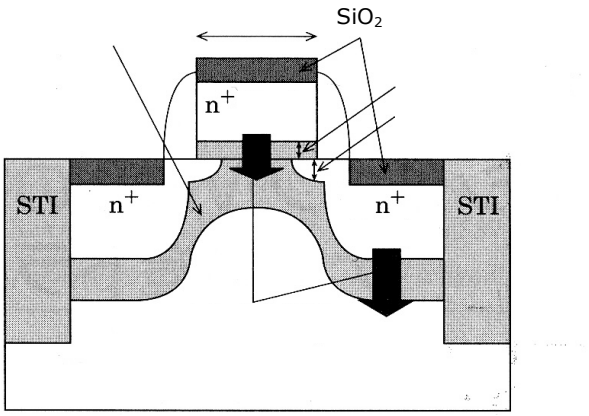
Field Effect Transistor (FET)

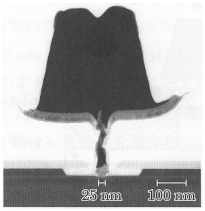
Metal / oxide / semiconductor (MOS) FET :

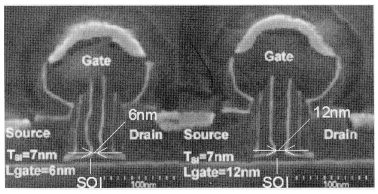




Miniaturisation of a MOSFET :







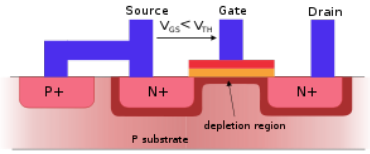
* http://www.wikipedia.org/

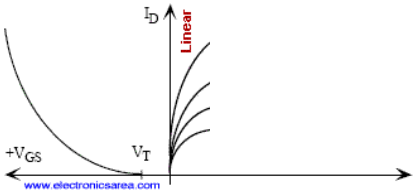
** H. Sakaki and N. Yokoyama, *Nanoelectronics* (Ohm-sha, Tokyo, 2004).

MOSFET

* https://www.youtube.com/watch?v=fCymWHssFIQ

MOSFET Operation

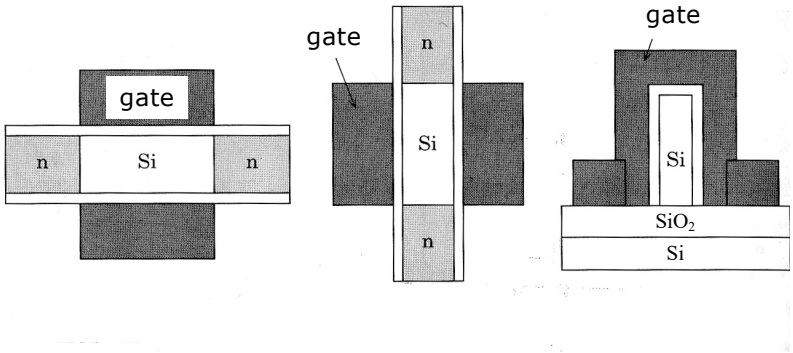




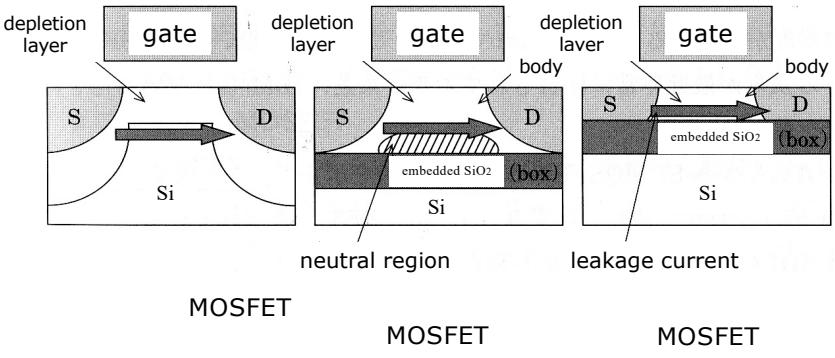
* http://www.wikipedia.org/
** http://www.electronicsarea.com/MOSFET_cutoff_linear_regions.asp

Improved MOSFET Structures

Double-gate structures :

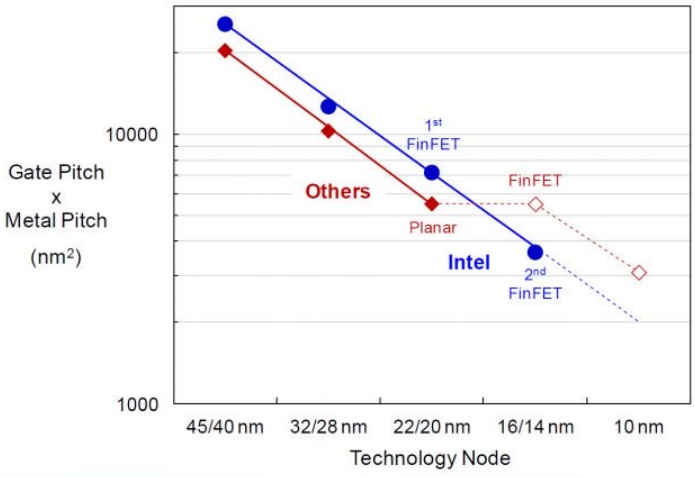


Improved depletion layers :



* H. Sakaki and N. Yokoyama, *Nanoelectronics* (Ohm-sha, Tokyo, 2004).

Logic Area Scaling

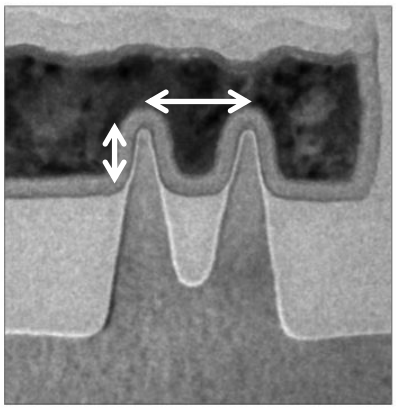


Others based on published information:

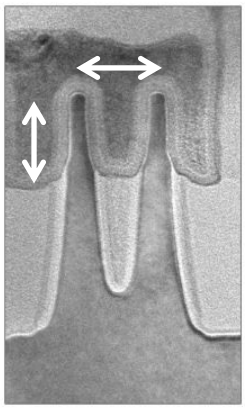
45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14

Intel is Shipping its 2nd Generation FinFETs Before Others Ship Their 1st Generation

Transistor Fin Improvement

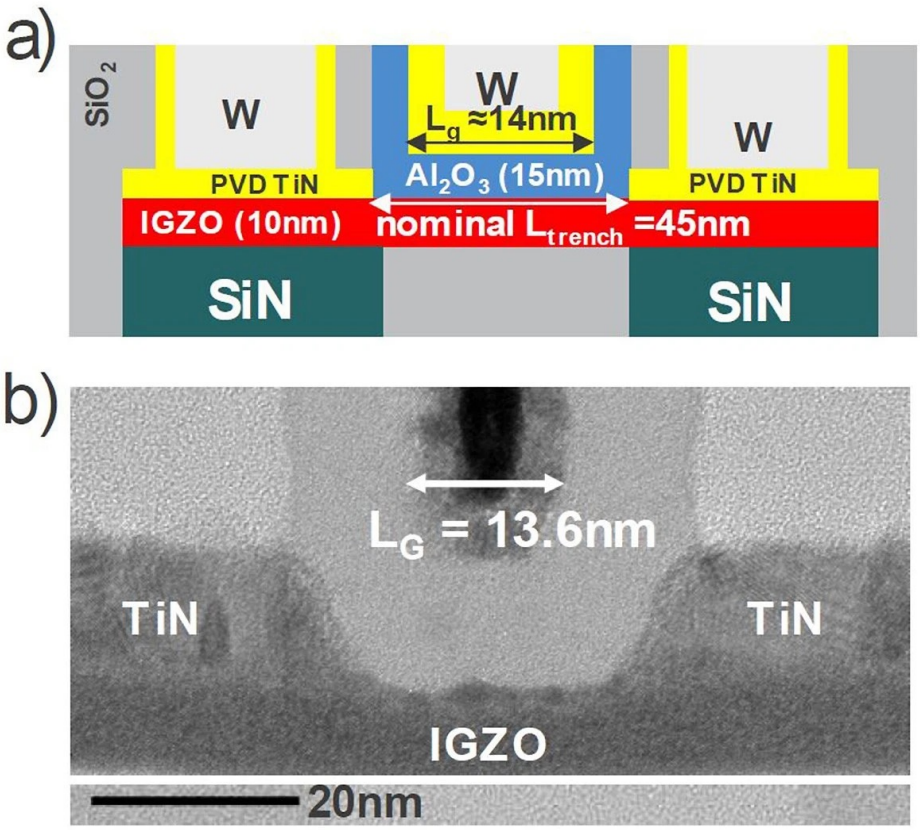


22 nm 1st Generation Tri-gate Transistor



14 nm 2nd Generation Tri-gate Transistor

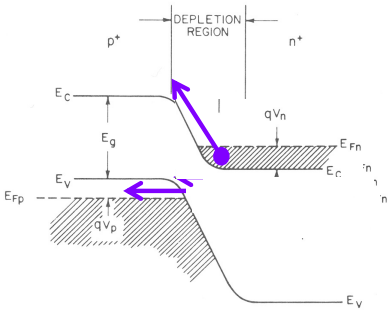
Latest Development with Indium-Gallium-Zinc-Oxide (IGZO)

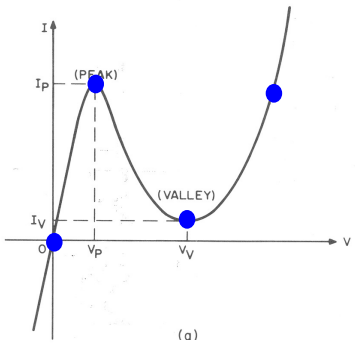


* https://www.eetimes.eu/capacitorless-dram-cell-on-igzo-base-shows-promising-values/

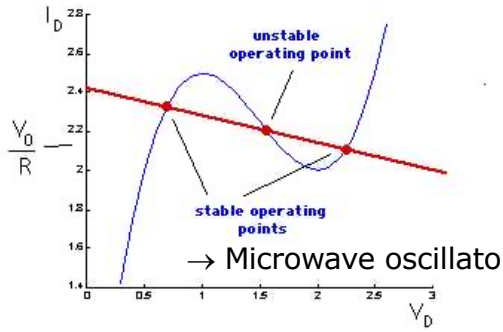
Esaki Diode

Tunnelling diode was invented by Leo Esaki in 1958 :





→ First observation of !

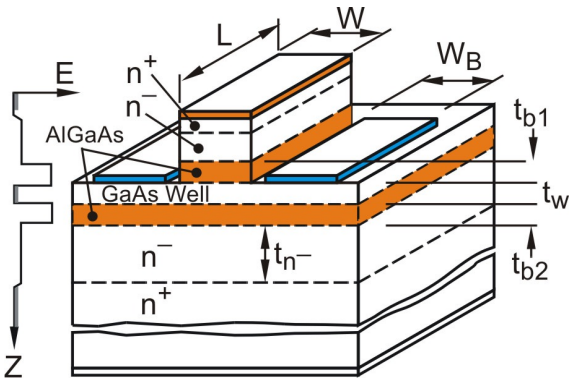


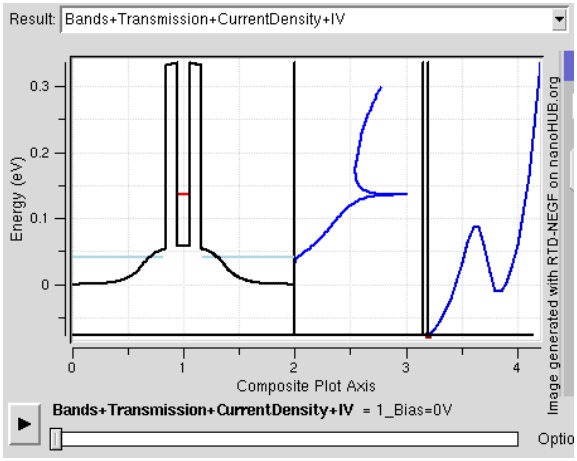
→ Microwave oscillator

* http://photos.aip.org/;
** S. M. Sze, *Physics of Semiconductor Devices* (John Wiley, New York, 1981).
*** http://www.geocities.jp/craft_3/Semiconductor/SONY_Transistor/sony_diode.html
† http://people.seas.harvard.edu/~jones/es154/lectures/lecture_2/load_line/load_line.html

Resonant Tunnelling Diode (RTD)

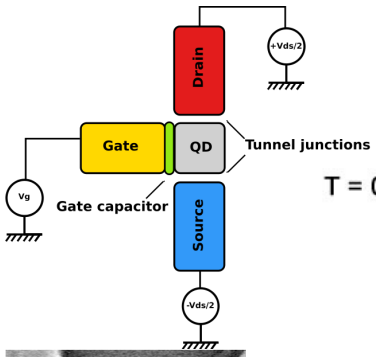
By forming a quantum well between tunnel barriers, resonant tunnelling is achieved.

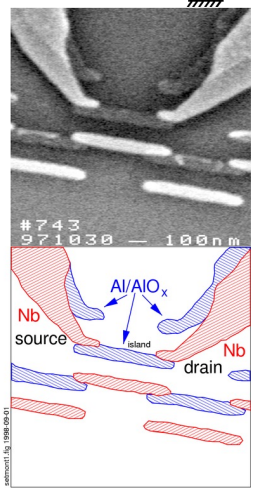


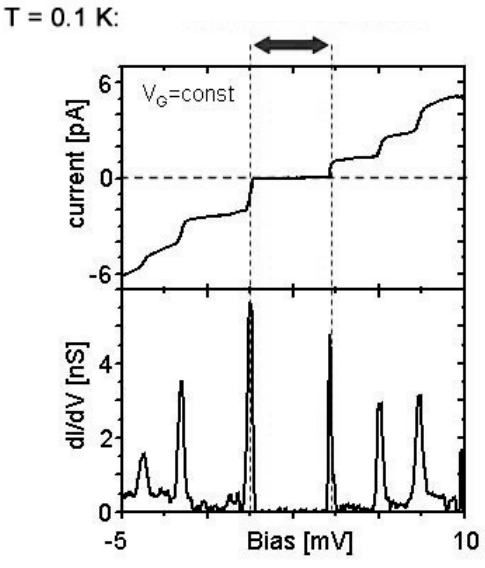


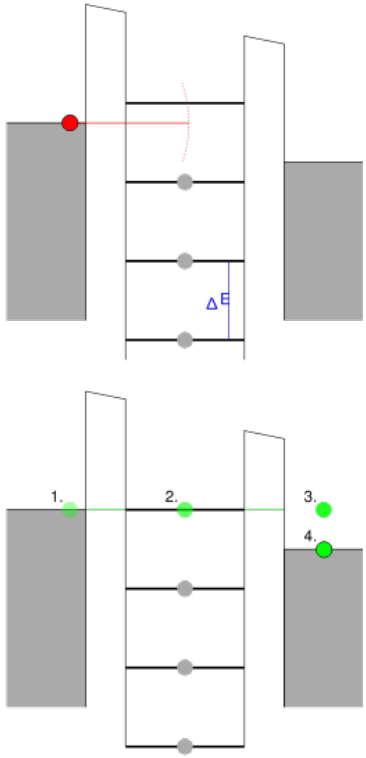
* http://www.hft.e-technik.uni-dortmund.de/forschung/projekt.php?id=8&lang=en
** http://nanohub.org/resources/8799

Coulomb Blockade and Co-Tunnelling



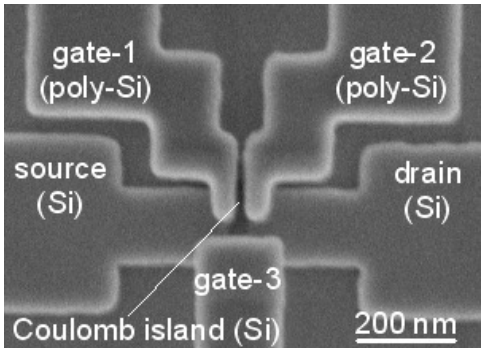


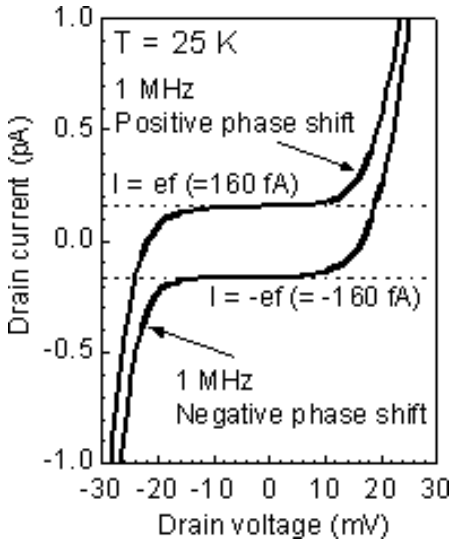




* http://www.wikipedia.org/
** http://people.ccmr.cornell.edu/~ralph/projects/metalset/index.html

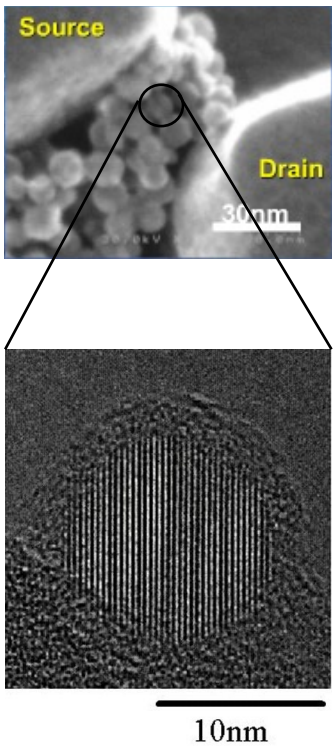
Single Electron Transistor (SET)

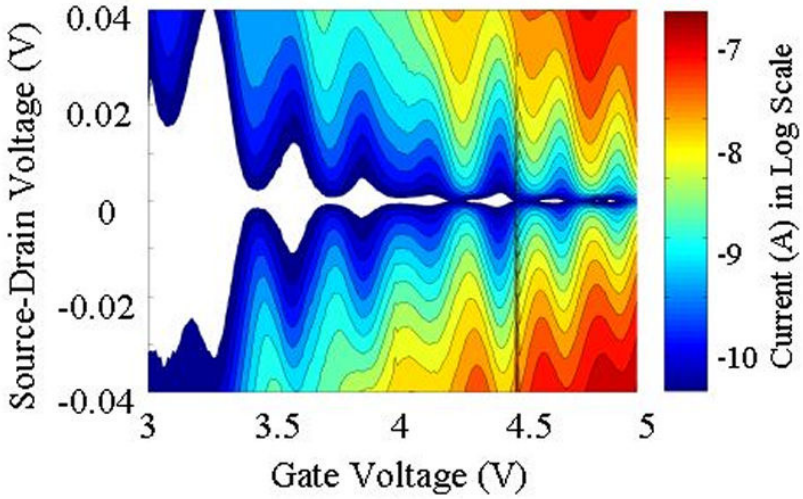




* http://www.brl.ntt.co.jp/J/activities/file/report02/J/report02.html

SET Operation





* http://odalab.pe.titech.ac.jp/en/

Energy Bands in Semiconductor Nanodevices

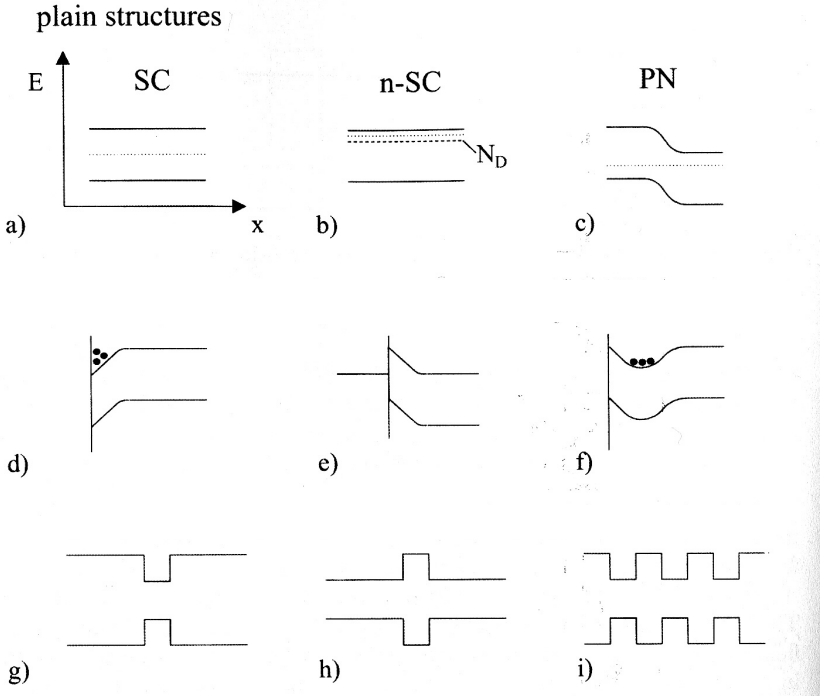
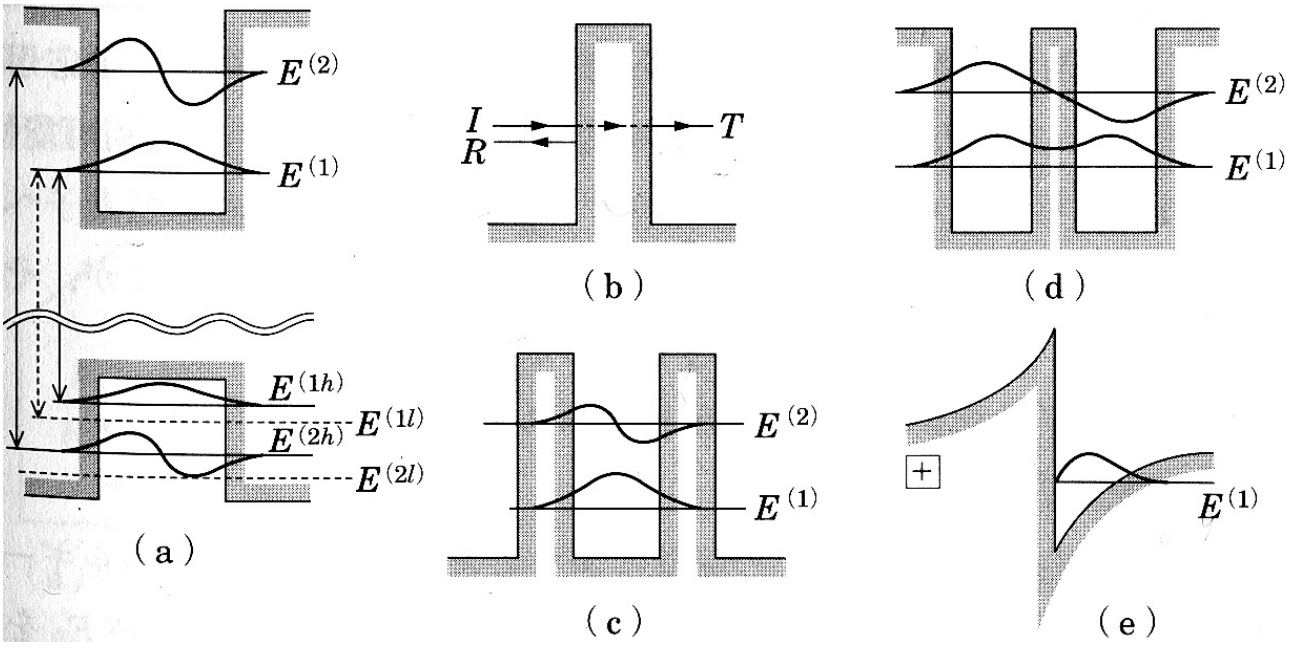


Fig. 2.3. Energy-band models of different semiconductor structures as they appear in devices: (a) semiconductor, (b) n-doped semiconductor, (c) pn-junction, (d) MOS structure with inversion layer, (e) Schottky contact, (f) MESFET, (g) quantum well, (h) quantum barrier, (i) superlattice

* K. Goser, P. Glosekotter and J. Diestuhl, *Nanoelectronics and Nanosystems* (Springer, Berlin, 2003).

Energy States in Semiconductor Nanodevices

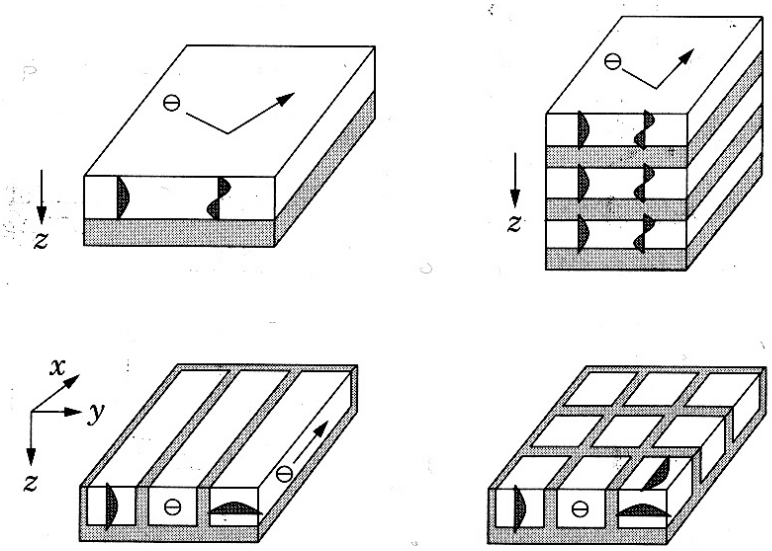
Eigen energy states in semiconductor nanodevices :



* H. Sakaki and N. Yokoyama, *Nanoelectronics* (Ohm-sha, Tokyo, 2004).

Standing Waves in Nanodevices

4 fundamental nano-device structures :



* H. Sakaki and N. Yokoyama, *Nanoelectronics* (Ohm-sha, Tokyo, 2004).

Josephson Junction

Superconductor / insulator / superconductor junction :

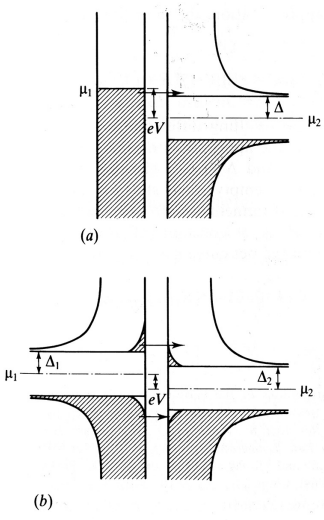
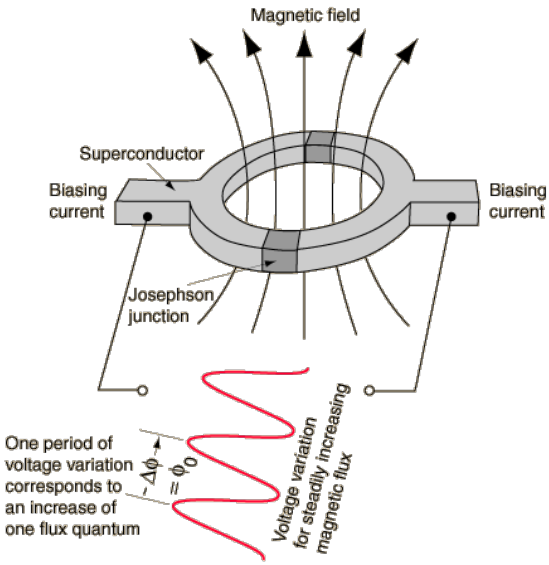


FIGURE 3.6
Example of semiconductor model description of electron tunneling. Density of states is plotted horizontally vs. energy vertically. Shading denotes states occupied by electrons. (*a*) *N*-*S* tunneling at $T = 0$, with bias voltage just above the conduction threshold, i.e., eV slightly exceeds the energy gap Δ. Horizontal arrow depicts electrons from the left tunneling into empty states on the right. (*b*) *S*-*S* tunneling at $T > 0$, with bias voltage below the threshold for conduction at $T = 0$, i.e., with $eV < \Delta_1 + \Delta_2$. Horizontal arrows depict tunneling involving thermally excited electrons or holes, respectively.

Cooper pairs in both superconductors can be represented by wavefunctions, of which phase difference generates a current across the junction.

Quantum phase → current

Superconducting quantum interference device (SQUID) :



→ sensor

* M. Tinkham, *Introduction to Superconductivity* (McGraw-Hill, New York, 1996);