Quick Review over the Last Lecture

Origin of magnetism:

(is equivalent to a ).

Dipole moment arrangement:

\[ \Theta (T_N) : \] temperature

\[ \Theta (T_C) : \] temperature
Contents of Nanoelectronics

I. Introduction to Nanoelectronics (01)
   01 Micro- or nano-electronics?

II. Electromagnetism (02 & 03)
   02 Maxwell equations
   03 Scholar and vector potentials

III. Basics of quantum mechanics (04 ~ 06)
   04 History of quantum mechanics 1
   05 History of quantum mechanics 2
   06 Schrödinger equation

IV. Applications of quantum mechanics (07, 10, 11, 13 & 14)
   07 Quantum well
   10 Harmonic oscillator
   11 Magnetic spin

V. Nanodevices (08, 09, 12, 15 ~ 18)
   08 Tunnelling nanodevices
   09 Nanomeasurements
   12 Spintronic nanodevices

12 Spintronic Nanodevices

- Magnetoresistance
- Hard disk drive
- Magnetic random access memory
- Spin-polarised three-terminal devices
Recent Progress in Magnetoelectronics I - Giant Magnetoresistance

Discovery of Giant Magnetoresistance

Giant magnetoresistance (GMR):
\[ [3 \text{ nm Fe} / 0.9 \text{ nm Cr}] \times 60 \]

50 % resistance change at 4.2 K

How Can We Find a Hard Disc Drive?

Open your computer ...

This is a HDD!

Do NOT Try This at Home!

Open a metal frame of a HDD ...

- Arm is operated by a linear motor with a very strong permanent magnet.
  - Arm moves ~ 100 times/sec.
  - Platter records data.
  - Platter rotates 5400 ~ 15000 rpm.
Where Can We Find a Hard Disc Drive?

Most popular recording media now:

- PC
- Hard disc recorder
- Video game
- Mobile phone
- Digital camera
- GPS navigation
- Video camera
- mp3 player

HDD Operation

* https://www.youtube.com/watch?v=NtPcoji21i0
Aerial Density Increase by GMR Introduction

Aerial density growth of hard disk drives:


Computer Operation

In a computer, data is transferred from a HDD to a Dynamic Random Access Memory:

Data stored in a capacitor.

→ Electric charge needs to be refreshed.
→ DRAM requires large power consumption.

* http://www.wikipedia.org/
Gap between HDD and DRAM

A gap between data storage and operation:

* http://agigatech.com/blog/page/2/

Flash Memory

In 1980, Fujio Masuoka invented a NOR-type flash memory:

- ✓ byte high-speed read-out
- × writing speed
- × Difficult to

Flash erase for a (1 ~ 10 kbyte) only!

In 1986, Fujio Masuoka invented a NAND-type flash memory:

- × No byte high-speed read-out
- ✓ writing speed
- ✓ Ideal for

* http://rikunabi-next.yahoo.co.jp/tech/docs/ct_s03600.jsp?p=000500
* http://www.wikipedia.org/
Solid State Drive with Flash Memory

Solid state drive (SSD) started to replace HDD:

pureSi introduced 2.5” 1-TB SDD in 2009:

- Data transfer speed at 300 MB/s
- Slow write speed

For example, a system with a units of 2kB for read / out and 256 kB for erase:
in order to write 1 bit, the worst case scenario is

- times read-out
- time flash erase
- times re-write

HDD vs Flash Memory

Demand for flash memories:

Price of flash memories:

* http://www.manifest-tech.com/ce_products/flash_revolution.htm
3D Flash Memory

3D NAND

1) Typical Planar NAND Cell String
2) Stretch It Out In The Middle
3) Fold It Over
4) Stand It Vertically

3D NAND Uses Less Wafer Area Than 2D For Same Bit Density

MRAM / Spin RAM as a Universal Memory

<table>
<thead>
<tr>
<th></th>
<th>Spin RAM</th>
<th>MRAM</th>
<th>FLASH</th>
<th>DRAM</th>
<th>FeRAM</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rules</td>
<td>32 nm</td>
<td>90 nm</td>
<td>32 nm</td>
<td>90 nm</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Non-volatility</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Read time</td>
<td>1 ns</td>
<td>&gt;10 ns</td>
<td>1 ns</td>
<td>10 ns</td>
<td>10 ns</td>
<td>N</td>
</tr>
<tr>
<td>Write time</td>
<td>1 ns</td>
<td>&gt;10 ns</td>
<td>1 ns</td>
<td>10 ns</td>
<td>10 ns</td>
<td>N</td>
</tr>
<tr>
<td>Repetition</td>
<td>&gt;10&lt;sup&gt;15&lt;/sup&gt;</td>
<td>&gt;10&lt;sup&gt;15&lt;/sup&gt;</td>
<td>&gt;10&lt;sup&gt;6&lt;/sup&gt;</td>
<td>&gt;10&lt;sup&gt;15&lt;/sup&gt;</td>
<td>&gt;10&lt;sup&gt;15&lt;/sup&gt;</td>
<td>&gt;10&lt;sup&gt;15&lt;/sup&gt;</td>
</tr>
<tr>
<td>Cell size</td>
<td>0.25 μm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>0.25 μm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>0.25 μm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>0.25 μm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>0.25 μm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>0.25 μm&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Cell density</td>
<td>5 Gb cm&lt;sup&gt;-2&lt;/sup&gt;</td>
<td>512 Mb cm&lt;sup&gt;-2&lt;/sup&gt;</td>
<td>512 Mb cm&lt;sup&gt;-2&lt;/sup&gt;</td>
<td>512 Mb cm&lt;sup&gt;-2&lt;/sup&gt;</td>
<td>512 Mb cm&lt;sup&gt;-2&lt;/sup&gt;</td>
<td>512 Mb cm&lt;sup&gt;-2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Chip capacity</td>
<td>&gt;1 Gb</td>
<td>&gt;1 Gb</td>
<td>&gt;1 Gb</td>
<td>&gt;1 Gb</td>
<td>&gt;1 Gb</td>
<td>&gt;1 Gb</td>
</tr>
<tr>
<td>Soft error hardness</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Process cost</td>
<td>RT process</td>
<td>Y</td>
<td>Lower bit cost</td>
<td>Y</td>
<td>Y</td>
<td>HT process</td>
</tr>
</tbody>
</table>

Note: * represents target values.

MRAM Applications

Improved MRAM Operation

Required writing currents for several techniques dependent upon cell size:

- Current-induced magnetisation reversal $J_c \sim 10^7 \text{ A/cm}^2$ (Current technology)
- Ampère-field-induced magnetisation reversal with a ferromagnetic overlayer (Current technology)
- Ampère-field-induced magnetisation reversal without a ferromagnetic overlayer (Current technology)
- Current-induced magnetisation reversal $J_c \sim 10^6 \text{ A/cm}^2$
- Current-induced magnetisation reversal $J_c \sim 5 \times 10^5 \text{ A/cm}^2$

Current-Induced Magnetisation Reversal

Anti-parallel (AP) ↔ parallel (P) reversal in a GMR / TMR junction:


Recent Progress in Magnetoelectronics II - Tunnel Magnetoresistance

Spin-Dependent Electron Tunneling

Jullière's model:

FM / insulator / FM junctions *

** TMR for Device Applications

Recent progress in TMR ratios:

> 400 % TMR ratio has been achieved!
> Gbit MRAM can be realised.

NOT following Jullière's model:**

\[ \text{TMR} = \frac{2P_1P_2}{(1 - P_1P_2)} \]

Improved Tunnel Barriers

Conventional amorphous barriers:

- Disorder at the interface:
  - FM over-oxidation
  - Lattice defects

- Defects in the barrier

Epitaxial (oriented) barriers:

- Latest MRAM

* After S. Yuasa et al., 28th Annual Conference on Magnetics, Sep. 21-24, 2004 (Okinawa, Japan).

Latest MRAM

* News from EverSpin, IBM and Toshiba.
Recent Progress in Spintronics


Spin-Polarised Three-Terminal Devices


<table>
<thead>
<tr>
<th>Interface</th>
<th>FM / SC hybrid Structures</th>
<th>Magnetic tunnel junctions (MTJ)</th>
<th>All metal and spin valve structures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spin carriers</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device applications</td>
<td>FM / 2DEG Schottky diodes</td>
<td>MOS junctions Coulomb blockade structures</td>
<td>Johnson transistors Spin valve transistors</td>
</tr>
<tr>
<td></td>
<td>Spin FET</td>
<td>SP-STM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Spin LED</td>
<td>Supercond. point contacts</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Spin RTD</td>
<td>Spin RTD</td>
<td></td>
</tr>
</tbody>
</table>

**Gate Voltage**

**Control**

**Input**

**Output**
## Major Spin-Polarised Three-Terminal Devices

<table>
<thead>
<tr>
<th></th>
<th>Spin FET</th>
<th>Spin LED</th>
<th>Spin RTD</th>
<th>Coulomb blockade</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td>Spin-polarised electrons / holes</td>
<td>Spin-polarised electrons / holes</td>
<td>Spin-polarised electrons / holes</td>
<td>Spin-polarised electrons</td>
</tr>
<tr>
<td><strong>Source</strong></td>
<td>Bias voltage</td>
<td>Bias voltage</td>
<td>Bias voltage</td>
<td>Bias voltage</td>
</tr>
<tr>
<td><strong>Gate</strong></td>
<td>Bias voltage</td>
<td>Bias voltage</td>
<td>Bias voltage</td>
<td>Bias voltage</td>
</tr>
<tr>
<td><strong>Drain</strong></td>
<td>Electrical signals - Spin-polarised electrons / holes</td>
<td>Circularly polarised electroluminescence (EL)</td>
<td>Circularly polarised electroluminescence (EL)</td>
<td>Electrical signals</td>
</tr>
<tr>
<td><strong>Notes</strong></td>
<td>• Low temperature • High magnetic field</td>
<td>• Low temperature</td>
<td>• Low temperature</td>
<td>• Low temperature</td>
</tr>
</tbody>
</table>

### Spin Valve / Magnetic Tunnel Transistors

- **Spin valve transistor**: *
- **Magnetic tunnel transistor**: †


Combining semiconductor with GMR / TMR devices:

→ First step towards all metal devices