Quick Review over the Last Lecture

**FeRAM:**

(a) Bit Line

(b) Bit Line

(c) Word Line

(d) Word Line

ITI/C type

IT type

**PRAM:**

**ReRAM:**

* http://loto.sourceforge.net/feram/doc/film.xhtml;
** http://www.wikipedia.org/;
Magnetotransport - Magnetism + Electronics

By taking advantages from both magnetism and semiconductor physics,

### Magnetism
- Atomically smooth surface / interface
- Spin diffusion length (∼)
- Low resistivity (Ω•m)
- Spin polarisation
- Magnetically anisotropic

### Semiconductor physics
- Depletion layer ( )
- Spin diffusion length (∼)
- Variable resistivity (Ω•m)
- Doping (atomic engineering)
- Isotropic
Conventional Electronics

Degenerating an electron state ...

Electrical current $e^-$

New degree of freedom: Spin
This review describes a new paradigm of electronics based on the spin degree of freedom of the electron. Either adding the spin degree of freedom to conventional charge-based electronic devices or using the spin alone has the potential advantages of nonvolatility, increased data processing speed, decreased electric power consumption, and increased integration densities compared with conventional semiconductor devices. To successfully incorporate spins into existing semiconductor technology, one has to resolve technical issues such as efficient injection, transport, control and manipulation, and detection of spin polarization as well as spin-polarized currents. Recent advances in new materials engineering hold the promise of realizing spintronic devices in the near future. We review the current state of the spin-based devices, efforts in new materials fabrication, issues in spin transport, and optical spin manipulation.

Until recently, the spin of the electron was ignored in mainstream charge-based electronics. A technology has emerged called spintronics (spin transport electronics or spin-based electronics), where it is not the electron charge but the electron spin that carries information, and this offers opportunities for a new generation of devices combining standard microelectronics with spin-dependent effects that arise from the interaction between spins of the carrier and the magnetic properties of the material.

Traditional approaches to using spin are based on the alignment of a spin (either “up” or “down”) relative to a reference (an applied magnetic field or magnetization orientation of the ferromagnetic film). Device operations then proceed with some quantity (electrical current) that depends in a predictable way on the degree of alignment. Adding the spin degree of freedom to conventional semiconductor charge-based electronics or using the spin degree of freedom alone will add substantially more capability and performance to electronic products. The advantages of these new devices would be nonvolatility, increased data processing speed, decreased electric power consumption, and increased integration densities compared with conventional semiconductor devices.

Major challenges in this field of spintronics that are addressed by experiment and theory include the optimization of electron spin lifetimes, the detection of spin coherence in nanoscale structures, transport of spin-polarized carriers across relevant length scales and heterointerfaces, and the manipulation of both electron and nuclear spins on sufficient-ly fast time scales. In response, recent experiments suggest that the storage time of quantum information encoded in electron spins may be extended through their strong interplay with nuclear spins in the solid state. Moreover, optical methods for spin injection, detection, and manipulation have been developed that exploit the ability to precisely engineer the coupling between electron spin and optical photons. It is envisioned that the merging of electronic, photonic, and magnetic technologies will ultimately lead to new spin-based multifunctional devices such as opto-FET (field-effect transistor), spin-LED (light-emitting diode), spin RTD (resonant tunneling device), optical switches operating at terahertz frequency, modulators, encoders, decoders, and quantum bits for quantum computation and communication. The success of these ventures depends on a deeper understanding of the fundamental spin interactions in solid state materials as well as the roles of dimensionality, defects, and semiconductor band structure in modifying these dynamics. If we can understand and control the spin...
Nano-Spintronic Devices

<table>
<thead>
<tr>
<th>Efffects</th>
<th>Interfaces</th>
<th>Magnetic tunnel junctions</th>
<th>FM/SC hybrid structures</th>
<th>Organic structures</th>
</tr>
</thead>
<tbody>
<tr>
<td>GMR</td>
<td>Ohmic contacts</td>
<td>TMR</td>
<td>Diodes</td>
<td>TMR/GMR</td>
</tr>
<tr>
<td>Difusive</td>
<td>Ballistic</td>
<td>Diffusive/ballistic (hot electrons)</td>
<td>Organic materials</td>
<td>Lateral spin valves</td>
</tr>
<tr>
<td>Spin media</td>
<td>Non-magnetic metals</td>
<td>Tunnel barriers</td>
<td>Semiconductors</td>
<td></td>
</tr>
<tr>
<td>Spin coherence</td>
<td>~ a few μm</td>
<td>MOS junctions</td>
<td>FET</td>
<td></td>
</tr>
<tr>
<td>Device applications</td>
<td>Johnson transistors</td>
<td>Coulomb blockade structures</td>
<td>Spin LED</td>
<td></td>
</tr>
<tr>
<td>Spin-valve transistors</td>
<td>Lateral spin valves</td>
<td>MRAM</td>
<td>Spin RTD</td>
<td></td>
</tr>
</tbody>
</table>

Theoretical Models for GMR

Interlayer exchange coupling model:
RKKY-like oscillation *

Two current model:
3d ferromagnets (FM) carry up spin current down spin current independently with different scattering rates at the FM layers the FM / NM interfaces. **

Current orientation:
Current in the plane (CIP) Current perpendicular to the plane (CPP)

Larger GMR Ratios

For > 2 Tb/in² recording:
Larger GMR ratios and smaller resistance-area product (RA) are required.

Spin-Dependent Electron Tunneling

Jullière's model:
FM / insulator / FM junctions

\[ E_1 = \mu_1 \]
\[ E_1 = 0 \]
\[ E_V \]
\[ E_2 = \mu_2 \]
\[ E_2 = 0 \]


Theoretical Models for TMR

Free electron models:
Juliiere's model:
\[
\begin{align*}
G^P & \propto a_1 a_2 + (1 - a_1)(1 - a_2) \\
G^{AP} & \propto a_1 (1 - a_2) + (1 - a_1)a_2
\end{align*}
\]
TMR ratio =

Slonczewski's model *:
spin split free electron band
\[ P = \]

WKB approximation **

Transfer Hamiltonian approach
Ab initio calculations

J. C. Slonczewski, Phys. Rev. B 39, 6995 (1989);
Improved Tunnel Barriers

Conventional amorphous barriers:

Disorder at the interface:
- FM over-oxidation
- lattice defects

Defects in the barrier:

Disorder at the interface:
- FM over-oxidation
- lattice defects
- island growth of the barrier

Epitaxial (oriented) barriers:

* After S. Yuasa et al., 28th Annual Conference on Magnetics, Sep. 21-24, 2004 (Okinawa, Japan).

TMR for Device Applications

Recent progress in TMR ratios:

> 600 % TMR ratio has been achieved!

> Gbit MRAM can be realised.

NOT following Jullière's model:

\[
TMR = \frac{2P_1P_2}{1 - P_1P_2}
\]

MRAM Cell

MRAM cell structure:

MRAM read-out:

MRAM Products

Freescale (now EverSpin Technologies) 4 Mbit MRAM:

* http://www.wikipedia.org/

* http://www.freescale.com/

Current-Induced Magnetisation Switching

Improved MRAM Operation (Spin RAM)

Required writing currents for several techniques dependent upon cell size:

- Current-induced magnetisation reversal with a ferromagnetic overlayer (Current technology)
  - $J_C \sim 10^7$ A/cm$^2$

- Ampère-field-induced magnetisation reversal with a ferromagnetic overlayer (Current technology)

- Ampère-field-induced magnetisation reversal without a ferromagnetic overlayer (Current technology)

Advantages of MRAM / Spin RAM

<table>
<thead>
<tr>
<th>Rules</th>
<th>Spin RAM</th>
<th>MRAM</th>
<th>FLASH</th>
<th>DRAM</th>
<th>FeRAM</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-volatility</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read time</td>
<td>~1 ns</td>
<td>300 ns (GMR)</td>
<td>10–50 ns</td>
<td>10–50 ns</td>
<td>10 ns</td>
<td>10–200 ns</td>
</tr>
<tr>
<td>Write time</td>
<td>&gt;10¹³</td>
<td>&lt;10 ns</td>
<td>0.1–100 ms</td>
<td>0.1–100 ms</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>Repetition</td>
<td>&gt;10¹⁵</td>
<td>&gt;10⁹</td>
<td>&gt;10⁹</td>
<td>&gt;10¹³</td>
<td>&gt;10¹³</td>
<td>10⁹–10¹²</td>
</tr>
<tr>
<td>Cell size</td>
<td>0.01 μm²</td>
<td>0.25 μm²</td>
<td>0.02 μm²</td>
<td>0.01 μm²</td>
<td>0.25 μm²</td>
<td>0.25 μm²</td>
</tr>
<tr>
<td>Cell density</td>
<td>5 Gb cm⁻²</td>
<td>256 Mb cm⁻²</td>
<td>2.5 Gb cm⁻²</td>
<td>512 Mb cm⁻²</td>
<td>256 Mb cm⁻²</td>
<td>64 Mb cm⁻²</td>
</tr>
<tr>
<td>Chip capacity</td>
<td>27 F²</td>
<td>4 F²</td>
<td>8 F²</td>
<td>8 F²</td>
<td>92 F²</td>
<td></td>
</tr>
<tr>
<td>Program energy</td>
<td>120 pJ</td>
<td>10 nJ</td>
<td>30–120 nJ</td>
<td>5 pJ + refresh</td>
<td>&lt;10 Mb</td>
<td>5 pJ</td>
</tr>
<tr>
<td>SOI error hardness</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Process cost</td>
<td>RT process</td>
<td>Lower bit cost</td>
<td>Y</td>
<td>Y</td>
<td>HT process</td>
<td></td>
</tr>
</tbody>
</table>

Note: * represents target values.


MRAM Operation

* https://www.youtube.com/watch?v=VRJ7xYPMfGA
Memory Types

Rewritable

Volatile

Dynamic

DRAM

SRAM

Non-volatile

Static

MRAM

FeRAM

PRAM

Read only

Non-volatile

Static

PROM

Mask ROM

Read majority (Writable)

Non-volatile

Static

Flash

EPROM

* http://www.semiconductorjapan.net/serial/lesson/12.html

STT-MRAM Products

In 2012, EverSpin Technologies introduced 64 Mbit MRAM:

* http://www.everspin.com/
STT-MRAM Advantages 1

**Delivering 10x better Price/Performance**

**Cloud Storage Needs:**
- More content & users, instant access
- Better response times from storage
- Predictable balanced performance

**Nanosecond-class MRAM Storage**

<table>
<thead>
<tr>
<th></th>
<th>NAND</th>
<th>MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>64Gb</td>
<td>1Gb</td>
</tr>
<tr>
<td>Latency</td>
<td>50us</td>
<td>45ns</td>
</tr>
<tr>
<td>4KB Write IOPS</td>
<td>800</td>
<td>400k</td>
</tr>
<tr>
<td>Cost/GB</td>
<td>1</td>
<td>50</td>
</tr>
</tbody>
</table>

* at only 50x Cost/GB

* http://www.everspin.com/

STT-MRAM Advantages 2

**Delivering 100x Power/Performance**

**Data Center needs:**
- Number of servers & CPU cores exploding
- Better bandwidth & IOPS to handle Big Data
- More performance @ less power to scale up

**High Performance, Power-Efficient MRAM Storage**

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<tbody>
<tr>
<td>Density</td>
<td>64Gb</td>
<td>1Gb</td>
</tr>
<tr>
<td>Power</td>
<td>80mW</td>
<td>400mW</td>
</tr>
<tr>
<td>4KB Write IOPS</td>
<td>800</td>
<td>400k</td>
</tr>
<tr>
<td>Cost/GB</td>
<td>1</td>
<td>50</td>
</tr>
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</table>

* at only 5x Power

* http://www.everspin.com/
Latest Spin RAM

* News from EverSpin, IBM and Toshiba.

MRAM for SRAM / DRAM Replacement

Magnetic sensor supply chain and key players*

*Non-exhaustive list of the magnetic sensor supply chain and its key players

MRAM Applications

* https://www.i-micronews.com/