HPC abbreviations and acronyms

ASCII American standard code for information interchange

ASIC Application-specific integrated circuit

BIOS Basic input/output system

BLAS Basic linear algebra subroutines

CAF Co-array Fortran

ccNUMA Cache-coherent nonuniform memory access

CFD Computational fluid dynamics

CISC Complex instruction set computer

CL Cache line

CPI Cycles per instruction

CPU Central processing unit

DDR Double data rate

DMA Direct memory access

DP Double precision

DRAM Dynamic random access memory

EPIC Explicitly parallel instruction computing

Flop Floating-point operation

FMA Fused multiply-add

FP Floating point

FPGA Field-programmable gate array

FSB Frontside bus

GCC GNU compiler collection

GPU Graphics processing unit

GUI Graphical user interface

HPC High performance computing

HT HyperTransport

IB InfiniBand

ILP Instruction-level parallelism

I/O Input/output

L1D Level 1 data cache

L1I Level 1 instruction cache

L2 Level 2 cache

L3 Level 3 cache

LD Load

MIMD Multiple instruction multiple data

MIPS Million instructions per second

MPI Message passing interface

MPMD Multiple program multiple data

MPP Massively parallel processing

NUMA Nonuniform memory access

OS Operating system

PC Personal computer

PCI Peripheral component interconnect

PGAS Partitioned global address space

POSIX Portable operating system interface for Unix

QPI QuickPath interconnect

RAM Random access memory

RISC Reduced instruction set computer

SIMD Single instruction multiple data

SISD Single instruction single data

SMP Symmetric multiprocessing

SMT Simultaneous multithreading

SP Single precision

SPMD Single program multiple data

SSE Streaming SIMD extensions

ST Store

STL Standard template library

TLB Translation lookaside buffer

UMA Uniform memory access

UPC Unified parallel C