TEXAS INSTRUMENTS

PCF8574

SCPS068J – JULY 2001 – REVISED MARCH 2015

PCF8574 Remote 8-Bit I/O Expander for I^{2}C Bus

1 Features

- Low Standby-Current Consumption of 10 µA Max
- I^{2}C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Telecom Shelters: Filter Units
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics
- Industrial Automation
- Products with GPIO-Limited Processors

3 Description

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I^{2}C) is designed for 2.5-V to 6-V V$_{CC}$ operation.
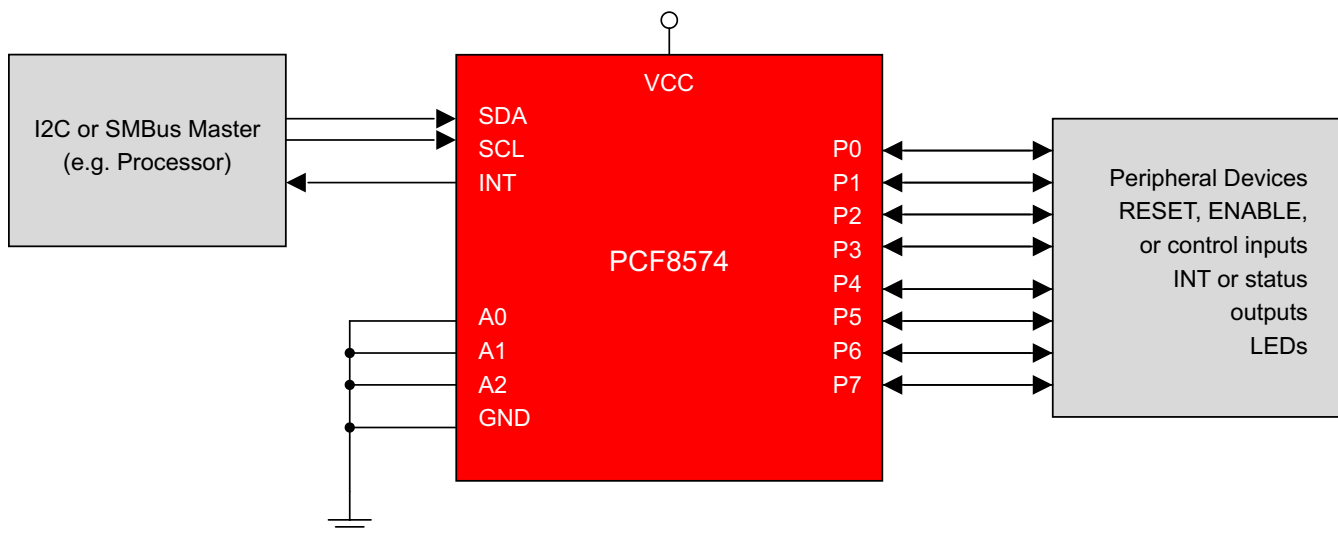
The PCF8574 device provides general-purpose remote I/O expansion for most microcontroller families by way of the I^{2}C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V$_{CC}$ is active.

Device Information[1]

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
PCF8574	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (16)	10.30 mm × 7.50 mm
	PDIP (16)	19.30 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	QFN (16)	3.00 mm × 3.00 mm
	VQFN (20)	4.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

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5 Pin Configuration and Functions

RGT PACKAGE
(TOP VIEW)

SDA SCL $\overline{INT}$ P7
16 15 14 13

V_{CC} 1 — 12 P6
A0 2 — 11 P5
A1 3 — 10 P4
A2 4 — 9 GND

5 6 7 8
P0 P1 P2 P3

RGY PACKAGE
(TOP VIEW)

$\overline{INT}$ P7
1 20

SCL 2 — 19 P6
NC 3 — 18 NC
SDA 4 — 17 P5
V_{CC} 5 — 16 P4
A0 6 — 15 GND
A1 7 — 14 P3
NC 8 — 13 NC
A2 9 — 12 P2

10 11
P0 P1

DGV OR PW PACKAGE
(TOP VIEW)

$\overline{INT}$ 1 — 20 P7
SCL 2 — 19 P6
NC 3 — 18 NC
SDA 4 — 17 P5
V_{CC} 5 — 16 P4
A0 6 — 15 GND
A1 7 — 14 P3
NC 8 — 13 NC
A2 9 — 12 P2
P0 10 — 11 P1

DW OR N PACKAGE
(TOP VIEW)

A0 1 — 16 V_{CC}
A1 2 — 15 SDA
A2 3 — 14 SCL
P0 4 — 13 $\overline{INT}$
P1 5 — 12 P7
P2 6 — 11 P6
P3 7 — 10 P5
GND 8 — 9 P4

Pin Functions

PIN					TYPE	DESCRIPTION
NAME	RGT	RGY	DGV or PW	DW or N		
A [0..2]	2, 3, 4	6, 7, 9	6, 7, 9	1, 2, 3	I	Address inputs 0 through 2. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
GND	9	15	15	8	—	Ground
$\overline{INT}$	14	1	1	13	O	Interrupt output. Connect to V_{CC} through a pullup resistor.
NC	-	3, 8, 13, 18	3, 8, 13, 18	-	—	Do not connect
P[0..7]	5, 6, 7, 8, 10, 11, 12, 13	10, 11, 12, 14, 16, 17, 19, 20	10, 11, 12, 14, 16, 17, 19, 20	4, 5, 6, 7, 9, 10, 11, 12	I/O	P-port input/output. Push-pull design structure.
SCL	15	2	2	14	I	Serial clock line. Connect to V_{CC} through a pullup resistor
SDA	16	4	4	15	I/O	Serial data line. Connect to V_{CC} through a pullup resistor.
V_{CC}	1	5	5	16	—	Voltage supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	V_{CC} + 0.5	V
V_O	Output voltage range[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{OK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±400	µA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−4	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	6	V
V_{IH}	High-level input voltage	$0.7 \times V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Low-level input voltage	−0.5	$0.3 \times V_{CC}$	V
I_{OH}	High-level output current		−1	mA
I_{OL}	Low-level output current		25	mA
T_A	Operating free-air temperature	−40	85	°C

6.4 Thermal Information

		PCF8574						UNIT
THERMAL METRIC[1]		DGV	DW	N	PW	RGT	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	16 PINS	20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	92	57	67	83	53	37	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

Product Folder Links: *PCF8574*

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.5 V to 6 V	−1.2			V
V_{POR}	Power-on reset voltage[2]	$V_I = V_{CC}$ or GND, $I_O = 0$	6 V		1.3	2.4	V
I_{OH}	P port	$V_O = $ GND	2.5 V to 6 V	30		300	µA
I_{OHT}	P port transient pullup current	High during acknowledge, $V_{OH} = $ GND	2.5 V		−1		mA
I_{OL}	SDA	$V_O = 0.4$ V	2.5 V to 6 V	3			mA
	P port	$V_O = 1$ V	5 V	10	25		
	$\overline{INT}$	$V_O = 0.4$ V	2.5 V to 6 V	1.6			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.5 V to 6 V			±5	µA
	$\overline{INT}$					±5	
	A0, A1, A2					±5	
I_{IHL}	P port	$V_I \geq V_{CC}$ or $V_I \leq$ GND	2.5 V to 6 V			±400	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, $f_{SCL} = 100$ kHz	6 V		40	100	µA
	Standby mode	$V_I = V_{CC}$ or GND, $I_O = 0$			2.5	10	
C_i	SCL	$V_I = V_{CC}$ or GND	2.5 V to 6 V		1.5	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
(2) The power-on reset circuit resets the I²C-bus logic with $V_{CC} < V_{POR}$ and sets all I/Os to logic high (with current source to V_{CC}).

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

		MIN	MAX	UNIT
f_{scl}	I²C clock frequency		100	kHz
t_{sch}	I²C clock high time	4		µs
t_{scl}	I²C clock low time	4.7		µs
t_{sp}	I²C spike time		100	ns
t_{sds}	I²C serial data setup time	250		ns
t_{sdh}	I²C serial data hold time	0		ns
t_{icr}	I²C input rise time		1	µs
t_{icf}	I²C input fall time		0.3	µs
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)		300	ns
t_{buf}	I²C bus free time between stop and start	4.7		µs
t_{sts}	I²C start or repeated start condition setup	4.7		µs
t_{sth}	I²C start or repeated start condition hold	4		µs
t_{sps}	I²C stop condition setup	4		µs
t_{vd}	Valid data time	SCL low to SDA output valid		3.4	µs
C_b	I²C bus capacitive load		400	pF

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 13)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pv}	Output data valid	SCL	P port		4	µs
t_{su}	Input data setup time	P port	SCL	0		µs
t_h	Input data hold time	P port	SCL	4		µs
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs

6.8 Typical Characteristics
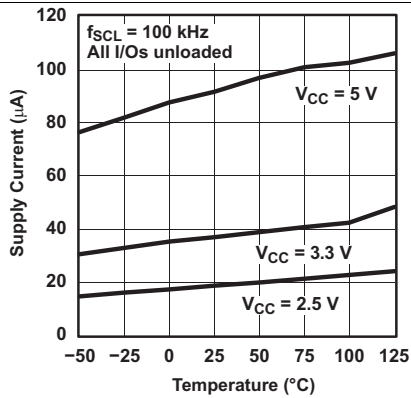
T_A = 25°C (unless otherwise noted)

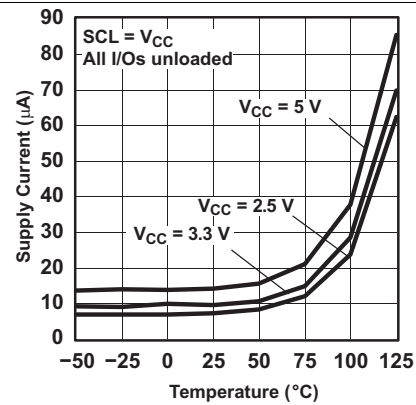Figure 1. Supply Current vs Temperature

Figure 2. Standby Supply Current vs Temperature
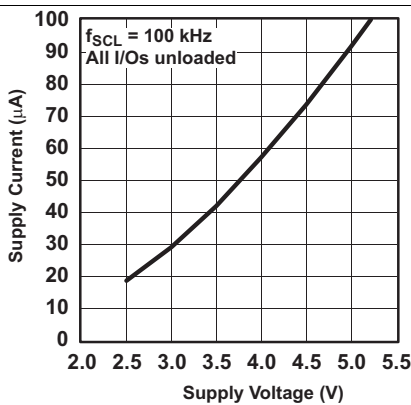
Figure 3. Supply Current vs Supply Voltage
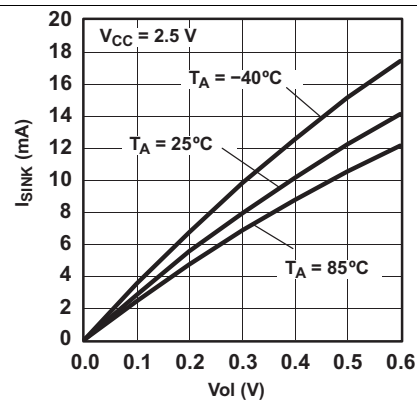
Figure 4. I/O Sink Current vs Output Low Voltage
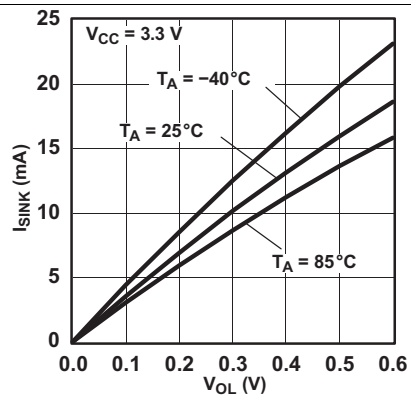
Figure 5. I/O Sink Current vs Output Low Voltage
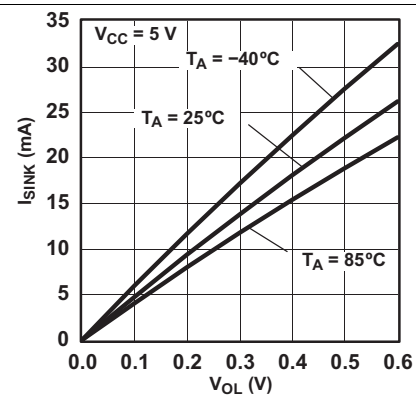
Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
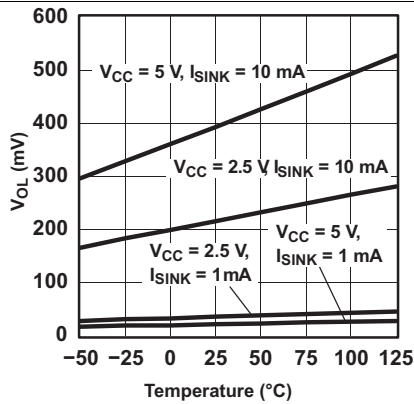
Figure 7. I/O Output Low Voltage vs Temperature
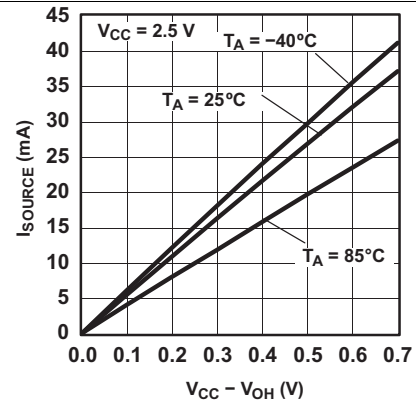
Figure 8. I/O Source Current vs Output High Voltage
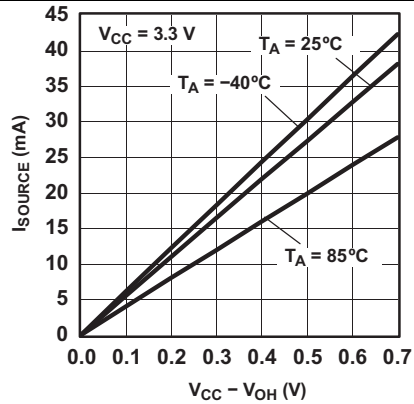
Figure 9. I/O Source Current vs Output High Voltage
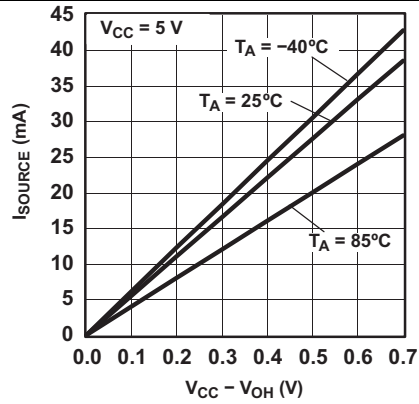
Figure 10. I/O Source Current vs Output High Voltage
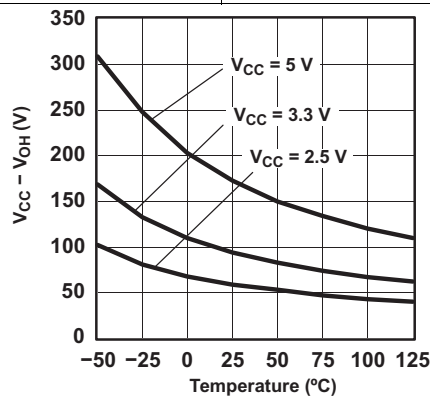
Figure 11. I/O High Voltage vs Temperature

7 Parameter Measurement Information
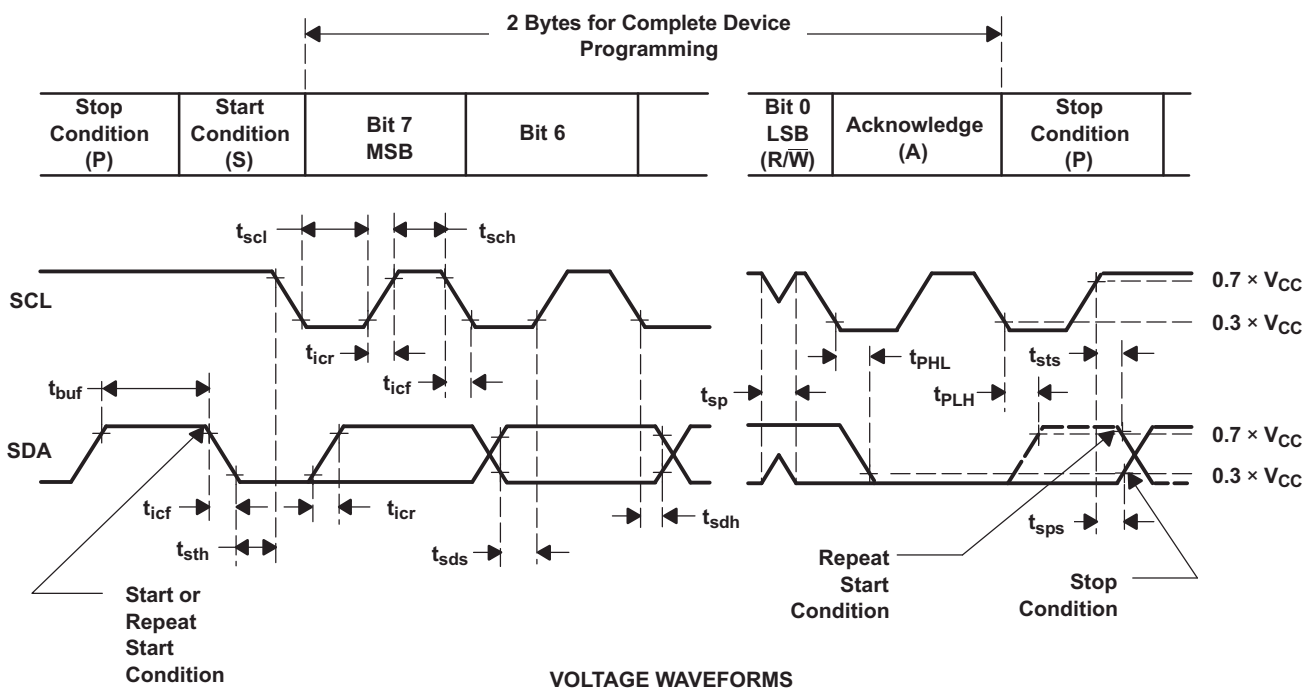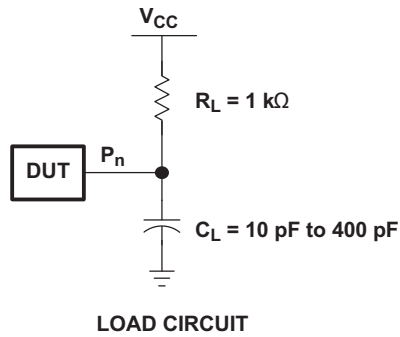
Figure 12. I²C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)
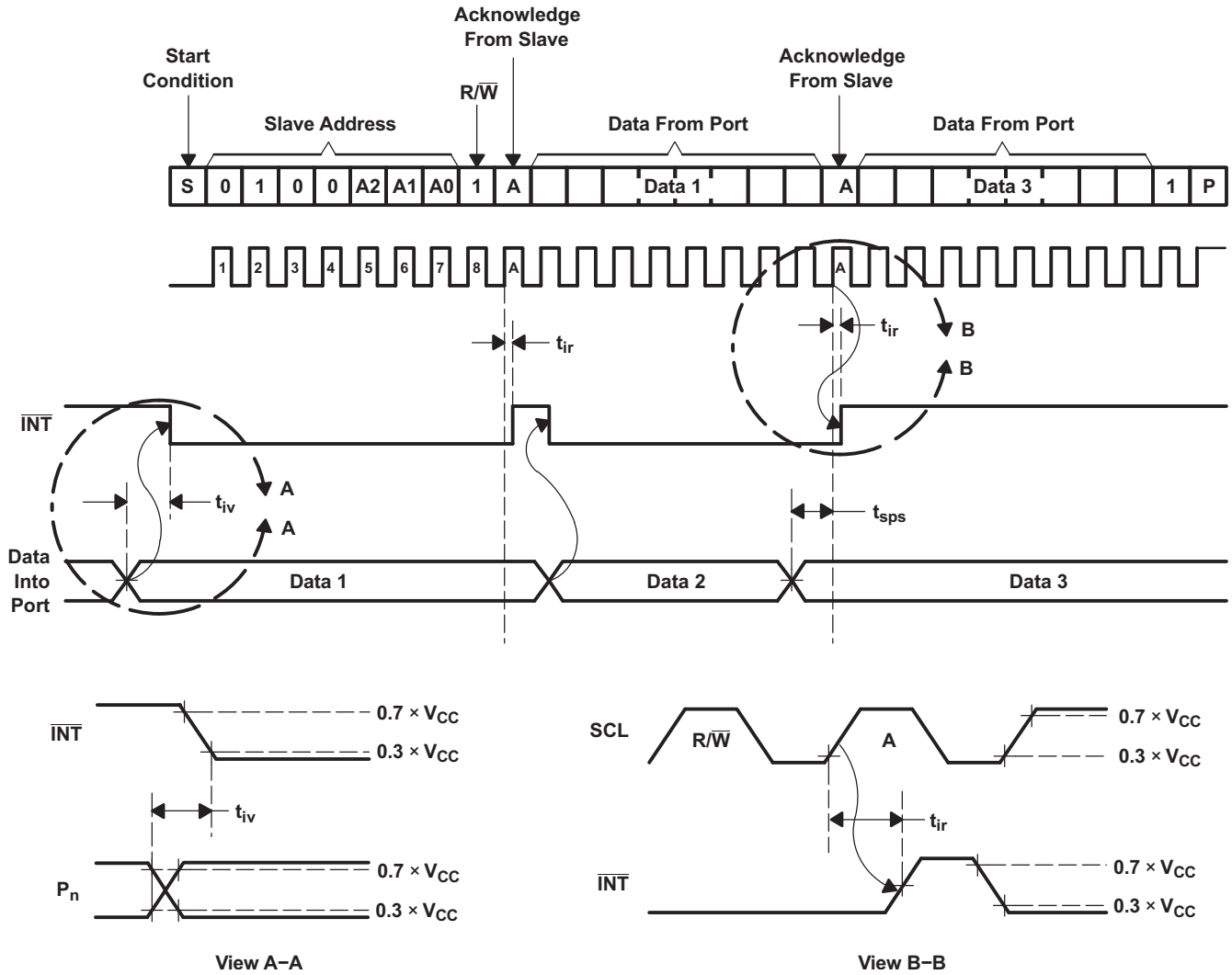
Figure 13. Interrupt Voltage Waveforms
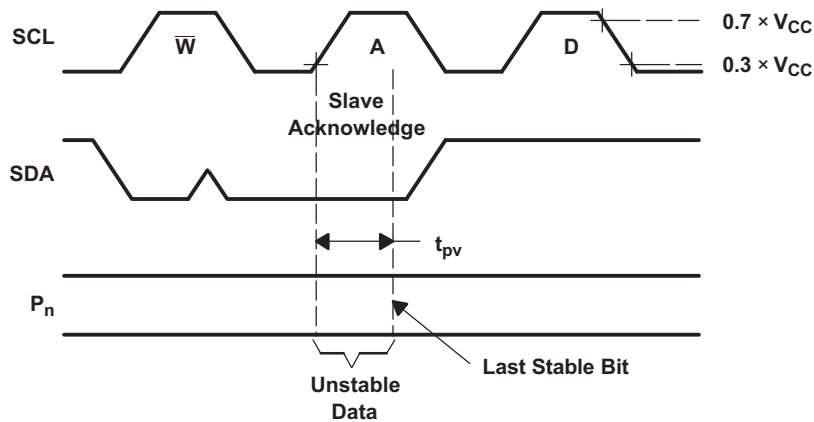
Figure 14. I²C Write Voltage Waveforms

Parameter Measurement Information (continued)

Figure 15. Load Circuits

Product Folder Links: *PCF8574*
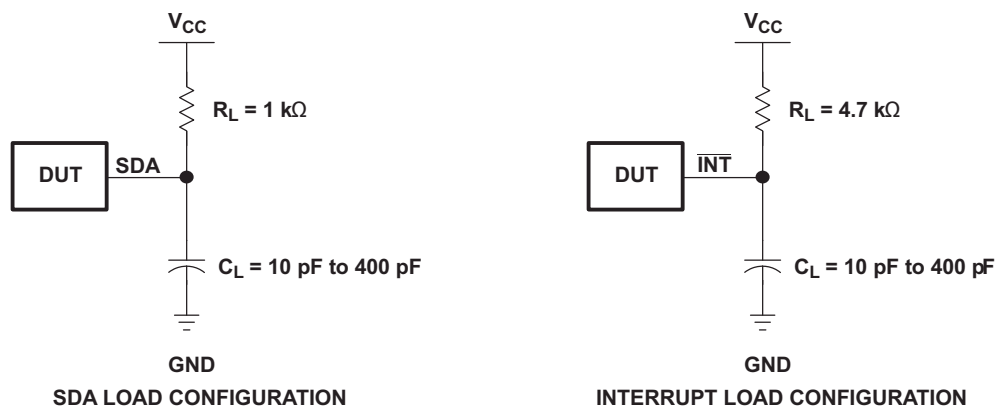
8 Detailed Description

8.1 Overview

The PCF8574 device is an 8-bit I/O expander for the two-line bidirectional bus (I2C) is designed for 2.5-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I2C interface (serial clock, SCL, and serial data, SDA, pins).

The PCF8574 device provides an open-drain output ($\overline{INT}$) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as $\overline{INT}$. Reading from, or writing to, another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see Figure 16 and Figure 17).

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate by way of the I²C bus. Therefore, PCF8574 can remain a simple slave device.

An additional strong pullup to V_{CC} allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

8.2 Functional Block Diagram

8.2.1 Simplified Block Diagram of Device
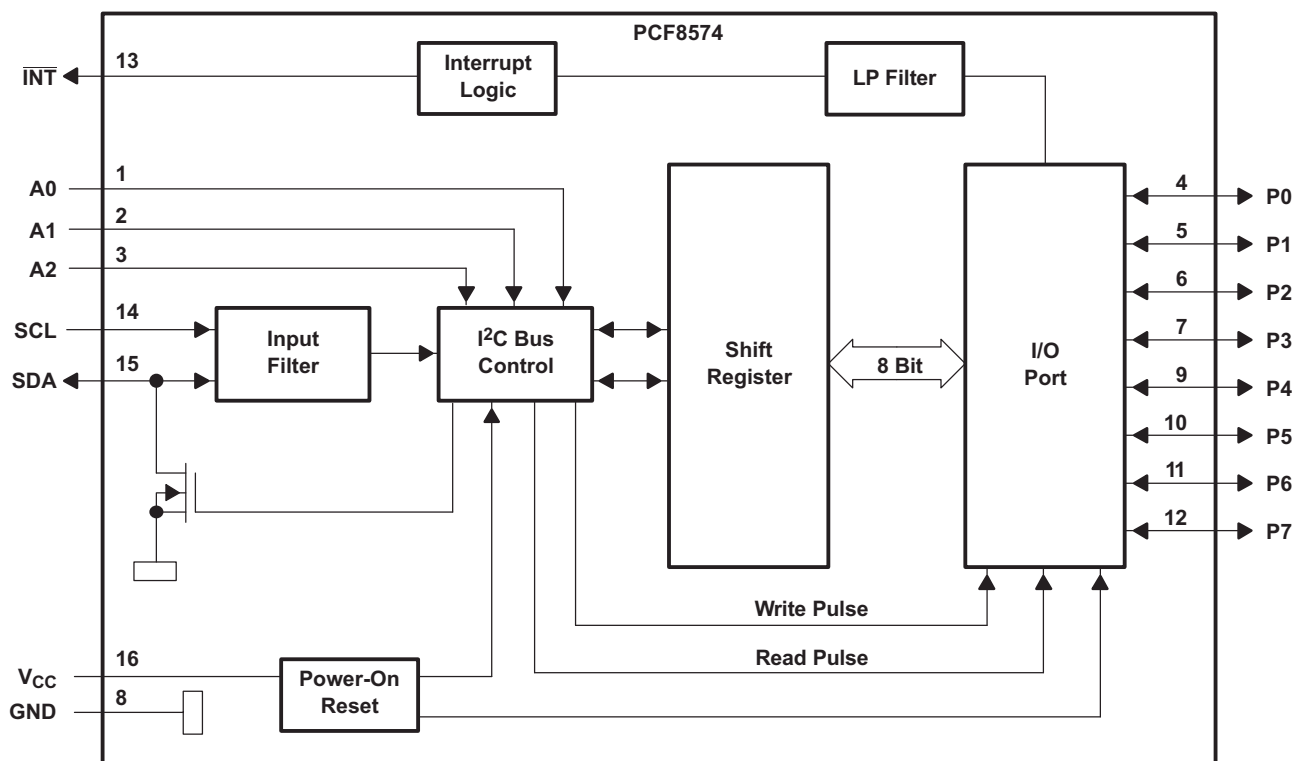
Pin numbers shown are for the DW and N packages.

Product Folder Links: *PCF8574*

Functional Block Diagram (continued)

8.2.2 Simplified Schematic Diagram of Each P-Port Input/Output
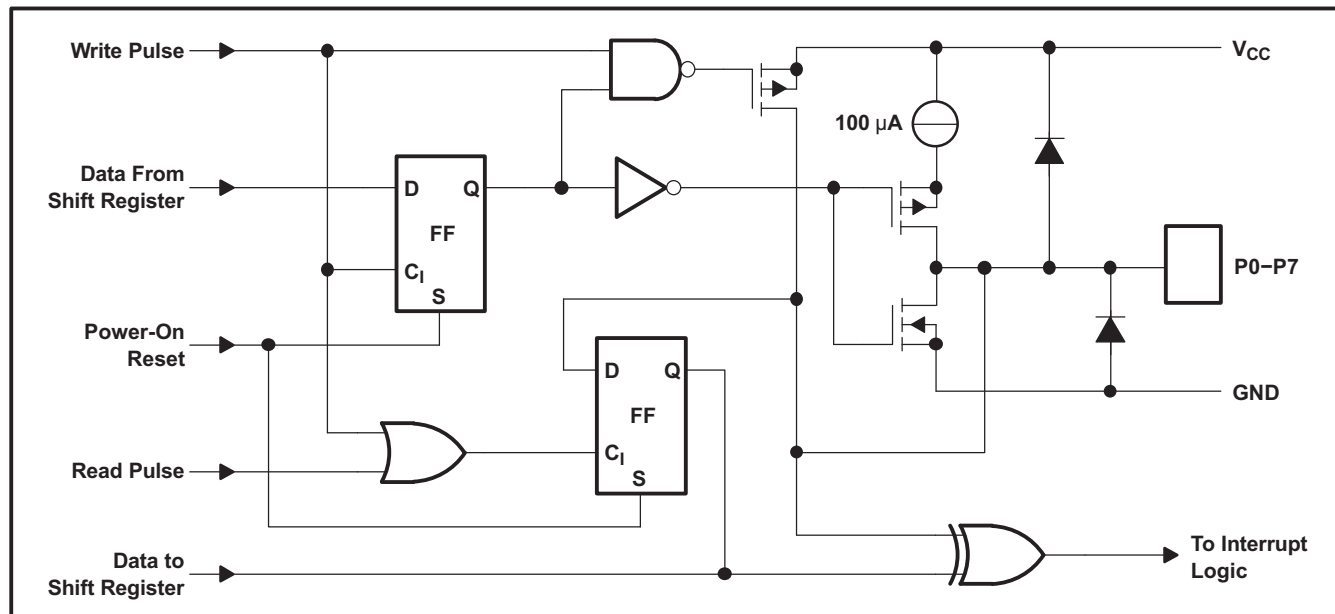
8.3 Feature Description

8.3.1 I^2C Interface

I^2C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/$\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/$\overline{W}$ bit is low, the data are from the master, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time, t_{pv}, after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master.

8.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.3.3 Address Reference

INPUTS			I²C BUS SLAVE 8-BIT READ ADDRESS	I²C BUS SLAVE 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

8.4 Device Functional Modes

Figure 16 and Figure 17 show the address and timing diagrams for the write and read modes, respectively.
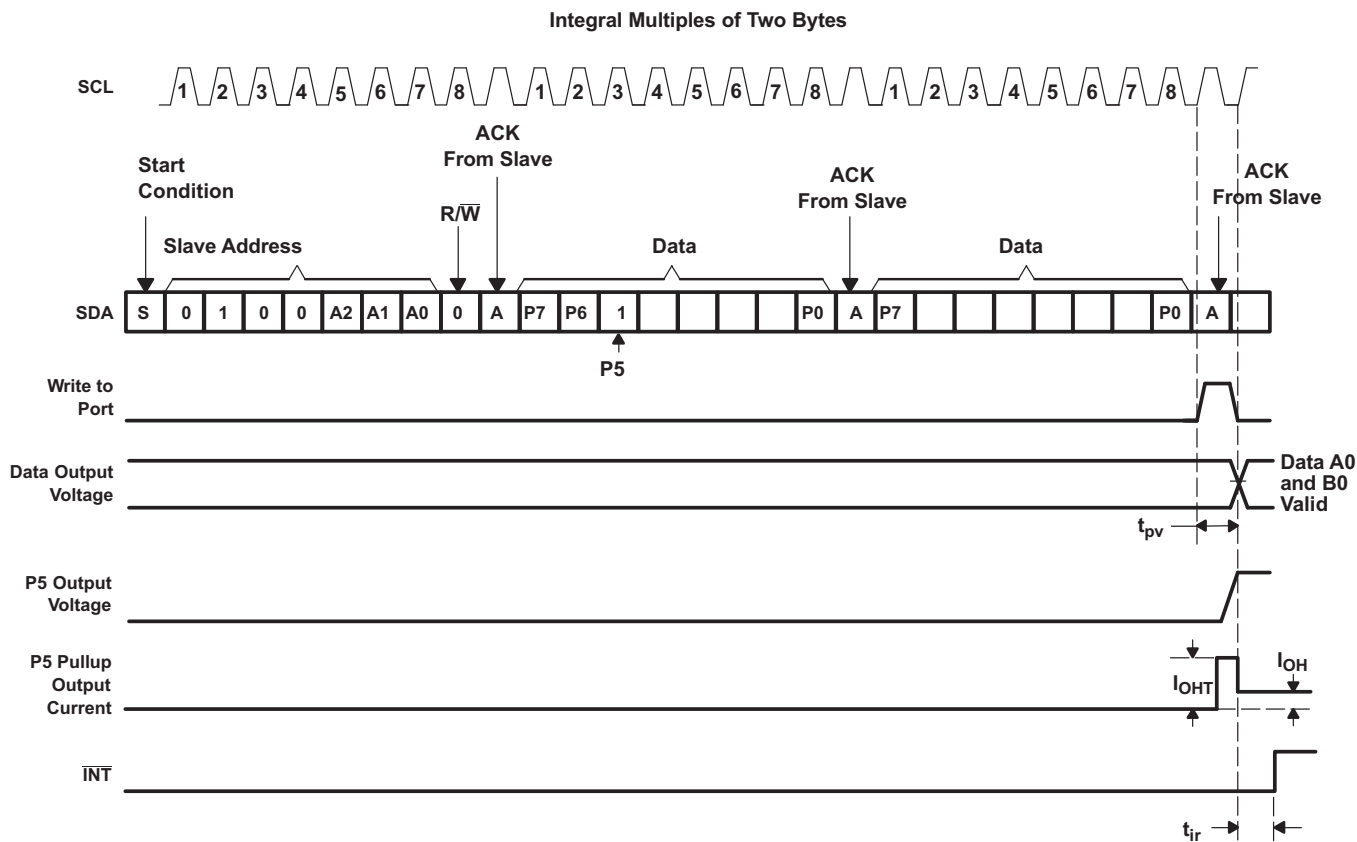
Figure 16. Write Mode (Output)

Device Functional Modes (continued)
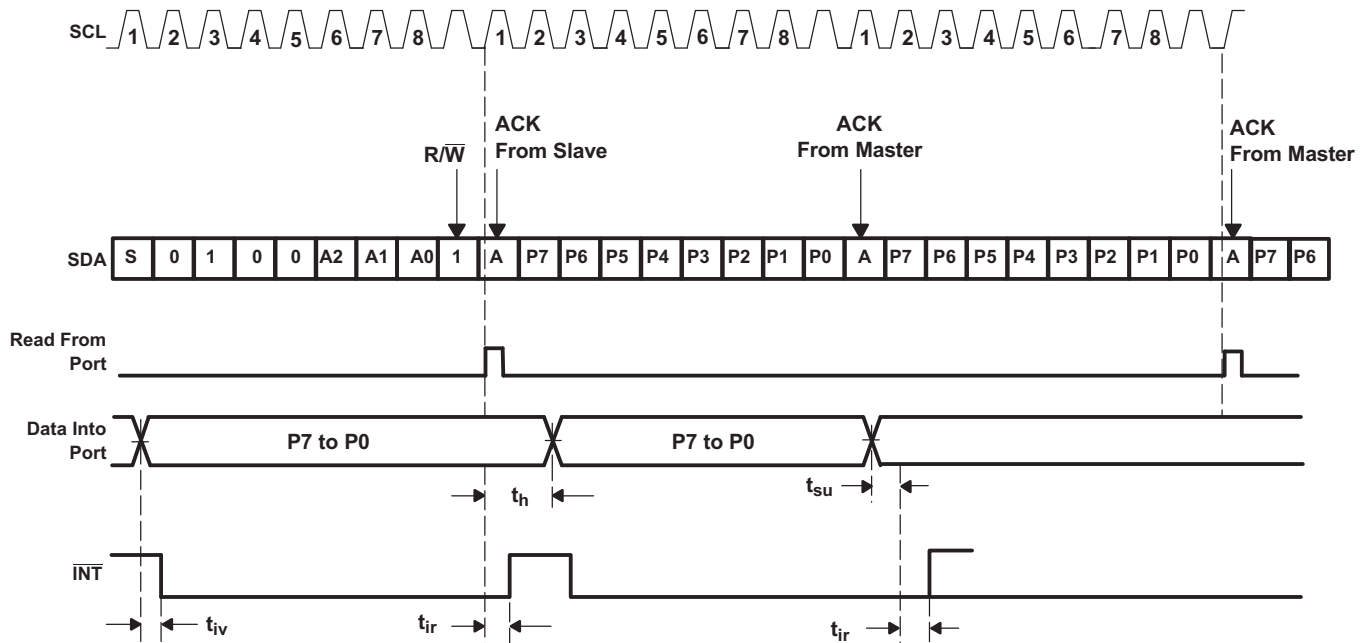
A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

Figure 17. Read Mode (Input)

Product Folder Links: *PCF8574*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 18 shows an application in which the PCF8574 device can be used.

9.2 Typical Application
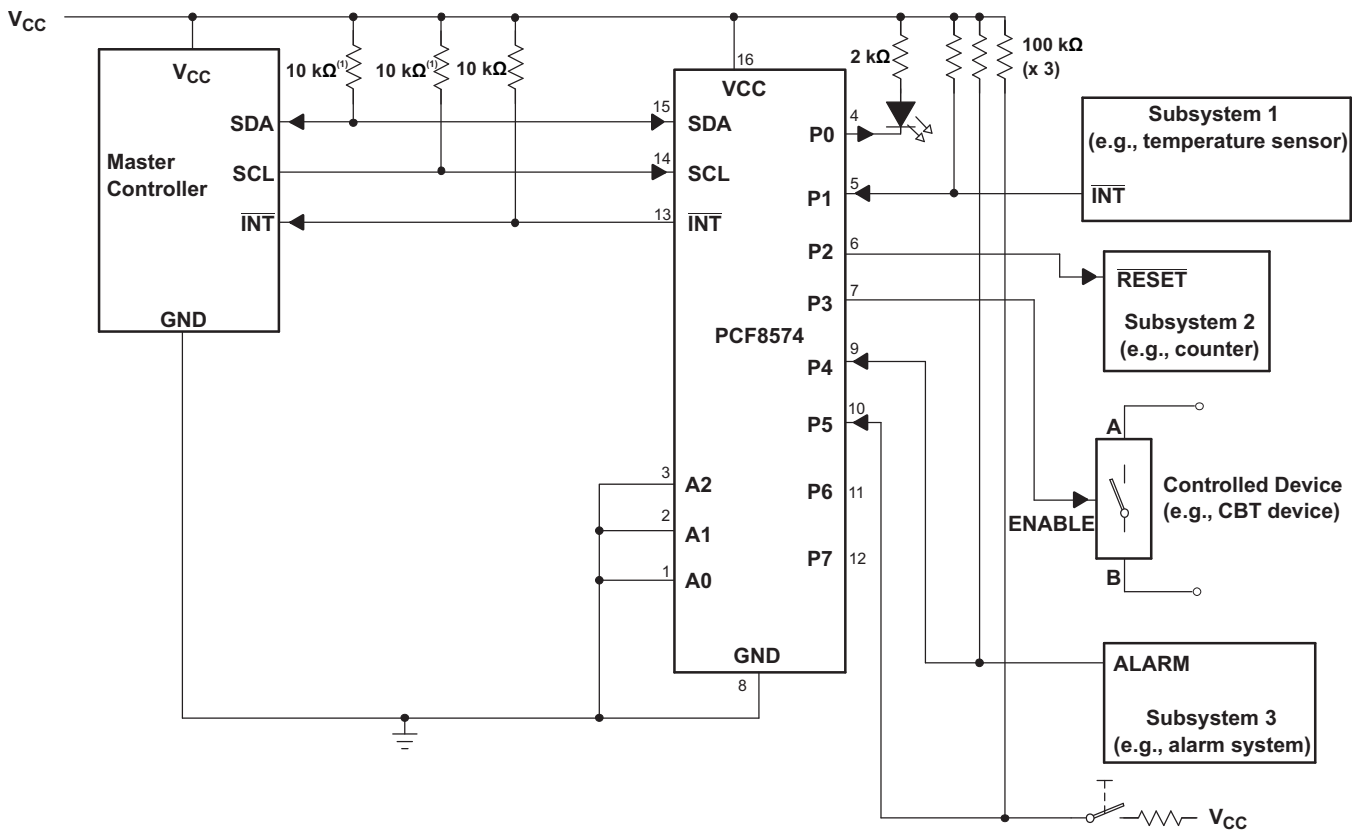
(1) The SCL and SDA pins must be tied directly to V_{CC} because if SCL and SDA are tied to an auxiliary power supply that could be powered on while V_{CC} is powered off, then the supply current, ICC, will increase as a result.

A. Device address is configured as 0100000 for this example.

B. P0, P2, and P3 are configured as outputs.

C. P1, P4, and P5 are configured as inputs.

D. P6 and P7 are not used and must be configured as outputs.

Figure 18. Application Schematic

Product Folder Links: *PCF8574*

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 18. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. Figure 19 shows a high-value resistor in parallel with the LED. Figure 20 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.
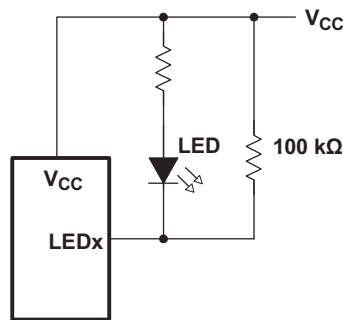
Figure 19. High-Value Resistor in Parallel With LED
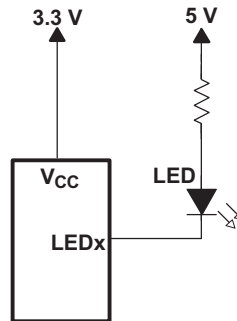
Figure 20. Device Supplied by a Lower Voltage

Product Folder Links: *PCF8574*

Typical Application (continued)

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^{2}C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}}$$

(1)

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$

(2)

The maximum bus capacitance for an I^{2}C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574 device, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

9.2.3 Application Curves

Standard-mode
(f_{SCL}= 100 kHz, t_r = 1 μs)

Fast-mode
(f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 21. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)

V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 22. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})
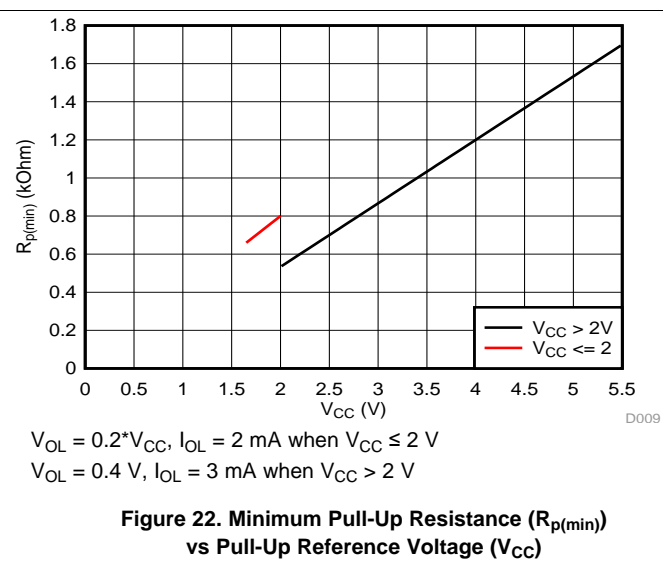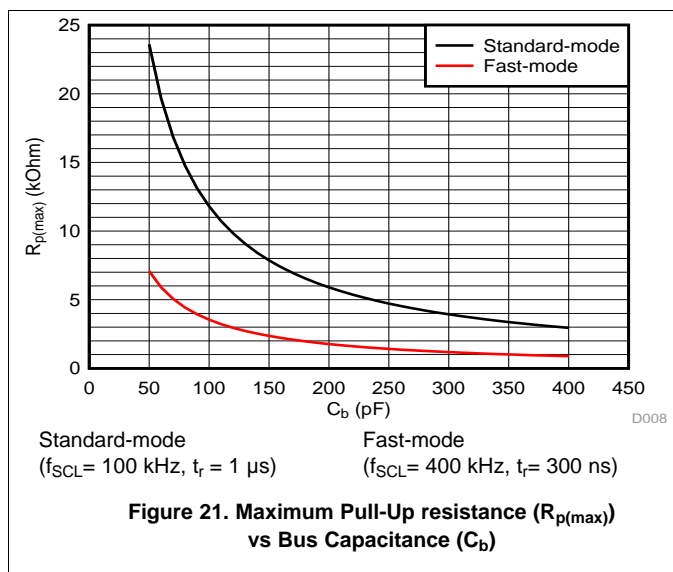
10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the PCF8574 device can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 23 and Figure 24.
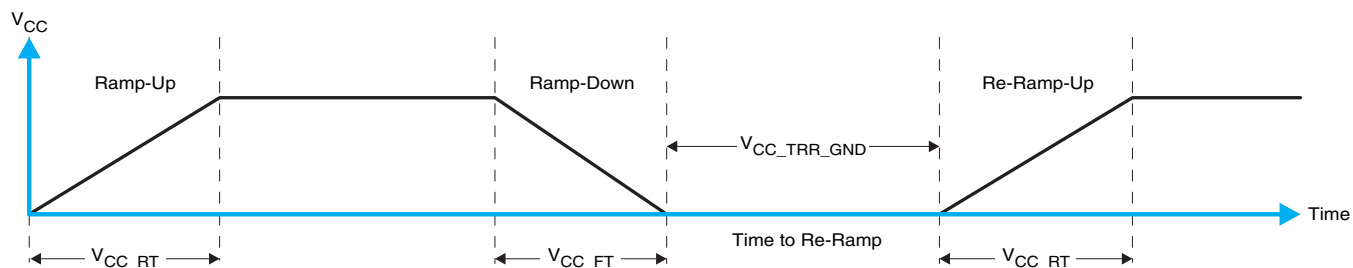
Figure 23. V$_{CC}$ is Lowered Below 0.2 V or 0 V and Then Ramped Up to V$_{CC}$
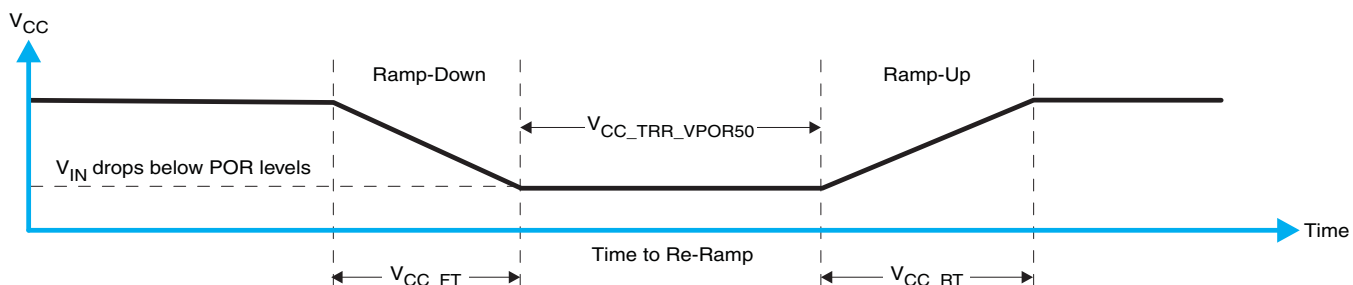
Figure 24. V$_{CC}$ is Lowered Below the POR Threshold, Then Ramped Back Up to V$_{CC}$

Table 1 specifies the performance of the power-on reset feature for PCF8574 for both types of power-on reset.

Table 1. Recommended Supply Sequencing and Ramp Rates[1]

PARAMETER			MIN	TYP	MAX	UNIT
V$_{CC\_FT}$	Fall rate	See Figure 23	1		100	ms
V$_{CC\_RT}$	Rise rate	See Figure 23	0.01		100	ms
V$_{CC\_TRR\_GND}$	Time to re-ramp (when V$_{CC}$ drops to GND)	See Figure 23	0.001			ms
V$_{CC\_TRR\_POR50}$	Time to re-ramp (when V$_{CC}$ drops to V$_{POR\_MIN}$ − 50 mV)	See Figure 24	0.001			ms
V$_{CC\_GH}$	Level that V$_{CCP}$ can glitch down to, but not cause a functional disruption when V$_{CCX\_GW}$ = 1 µs	See Figure 25			1.2	V
V$_{CC\_GW}$	Glitch width that will not cause a functional disruption when V$_{CCX\_GH}$ = 0.5 × V$_{CCx}$	See Figure 25				µs
V$_{PORF}$	Voltage trip point of POR on falling V$_{CC}$			0.767	1.144	V
V$_{PORR}$	Voltage trip point of POR on fising V$_{CC}$			1.033	1.428	V

(1) T$_A$ = −40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 25 and Table 1 provide more information on how to measure these specifications.
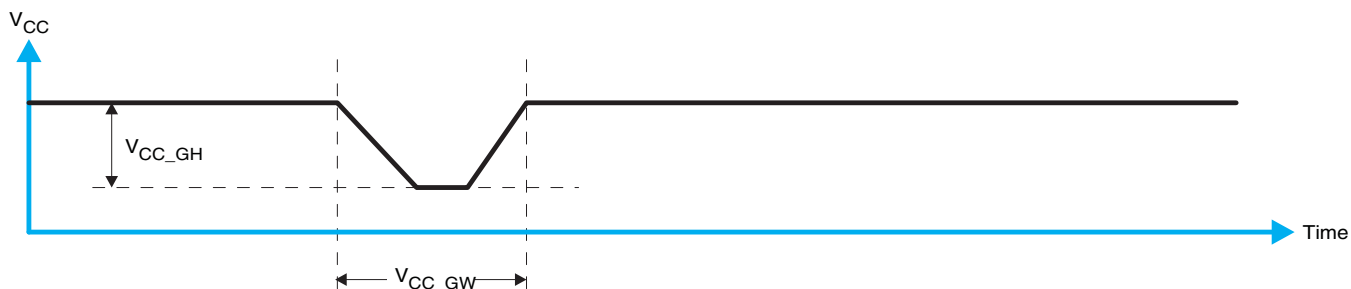
Figure 25. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 26 and Table 1 provide more details on this specification.

Figure 26. V_POR

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8574 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574 device as possible. These best practices are shown in Figure 27.

For the layout example provided in Figure 27, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 27.

11.2 Layout Example
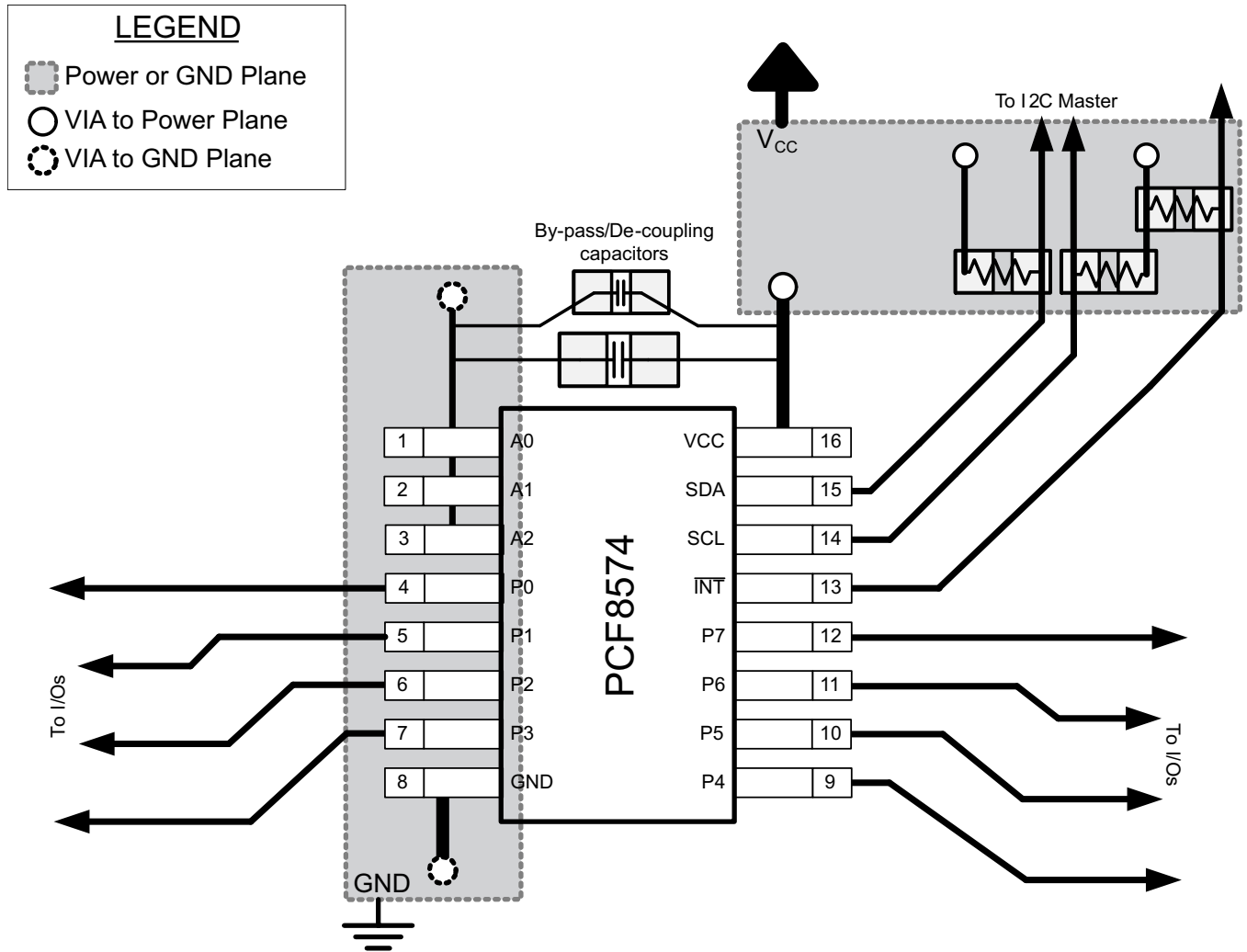
Figure 27. Layout Example for PCF8574

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Product Folder Links: *PCF8574*

30-Apr-2016

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574DGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574N	Samples
PCF8574NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574N	Samples
PCF8574PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWJ	Samples
PCF8574RGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574RGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8574DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8574DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCF8574DWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCF8574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCF8574RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
PCF8574RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8574DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
PCF8574DWR	SOIC	DW	16	2000	367.0	367.0	38.0
PCF8574DWRG4	SOIC	DW	16	2000	367.0	367.0	38.0
PCF8574PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PCF8574RGTR	QFN	RGT	16	3000	346.0	346.0	35.0
PCF8574RGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

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