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NERVOUS SYSTEMS

Neuromorphic Hardware Overview

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What is “Neuromorphic” Hardware?

NEURO: “RELATING TO NERVES OR THE NERVOUS SYSTEM”
MORPHIC: “OF OR PERTAINING TO FORM”

- **Term coined by Carver Mead in 1990[1], referring to analogue VLSI mimicking biological neural systems.**
- **The original idea of Brain-like computing is much older, discussed by Alan Touring[2] and John von Neumann[3] in the 1950’s.**
- **Neuromorphic systems are typically based on some combination of:**
  - **analogue data processing**
  - **asynchronous communication**
  - **massively parallel information processing**
  - **spiking-based information representation**
  - **collocating memory and processing**
  - **efficient, robust, low-power**

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Neuromorphic vs von Neumann

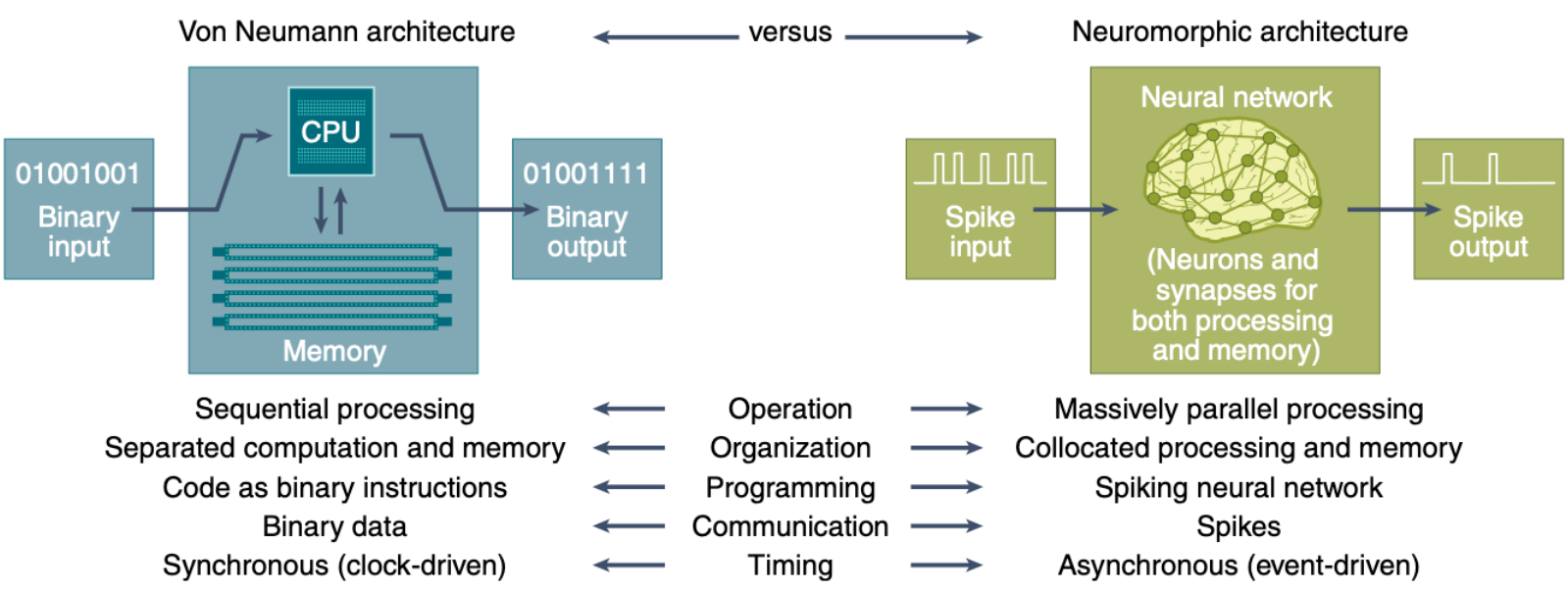

Image from [16] Schuman, Catherine D., Shruti R. Kulkarni, Maryam Parsa, J. Parker Mitchell, Prasanna Date, and Bill Kay. 2022. "Opportunities for Neuromorphic Computing Algorithms and Applications." Nature Computational Science 2 (1): 10–19.

Why Neuromorphic Hardware?

1980's Parallelism[4-6]
Simple processing elements, densely connected (Brain inspired).

von Neumann bottleneck

1990's Real-time Comp[10-11]
(Autonomous) robot control, image reconstruction, parallelism for application performance.

End of Dennard scaling

2010's Low-power[13]
20W Brain power, no A2D/D2A, AI/ML for edge applications.

1990's Computation Speed[7-9]
Inherent parallelism, machine learning acceleration with custom HW.

New devices and materials

late 1990's Robustness[4,12]
Inherent fault-tolerance, capability for HW to adapt and self-heal, advantage when dealing with intrinsic variability of novel devices.

Deep learning "AI"

All-time goals[14-16]**:**
- **Scalability**
- **von Neumann bottleneck (in-memory computing)**
- **Autonomous – online learning**
- **Neuroscience**

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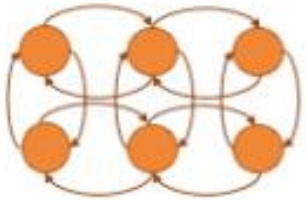
Designing Neuromorphic HW Systems

NETWORK TOPOLOGY AND HARDWARE MAPPING

Feed-forward

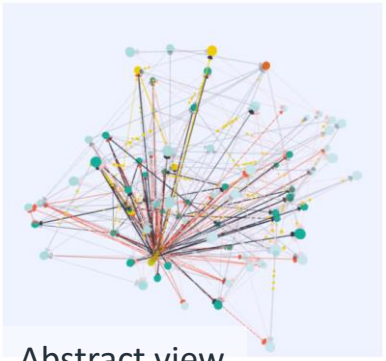
Feed-forward
with some recurrence

Sparsely-connected
Recurrent



Locally-connected
Recurrent

Fully-connected
Recurrent



Abstract view

Hardware mapping

Illustrations from [15] Schuman, Catherine D., Thomas E. Potok, Robert M. Patton, J. Douglas Birdwell, Mark E. Dean, Garrett S. Rose, and James S. Plank. 2017. “A Survey of Neuromorphic Computing and Neural Networks in Hardware.” arXiv [cs.NE]. arXiv. http://arxiv.org/abs/1705.06963.

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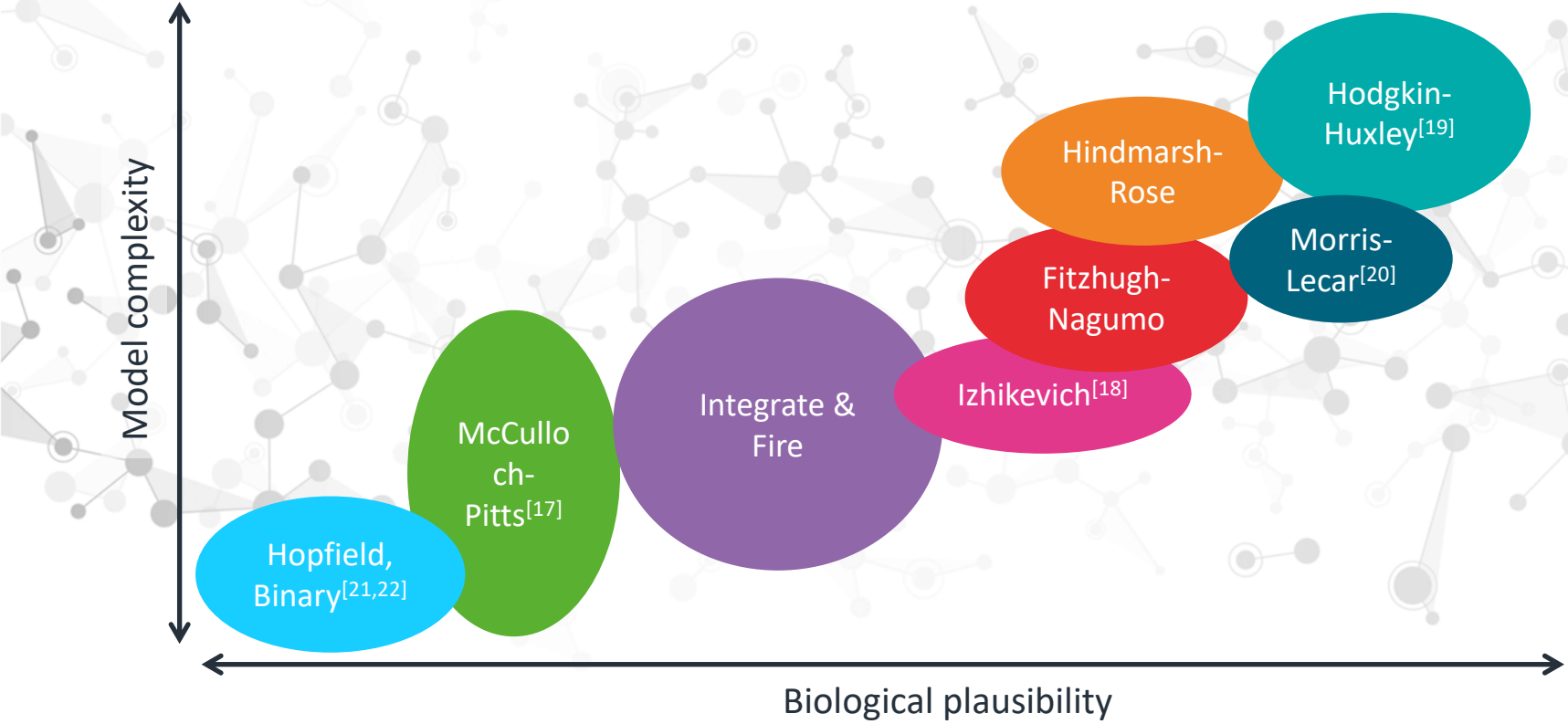
Neuron (& Synapse) Models

BIO-INSPIRED COMPUTATION MODEL ABSTRACTIONS



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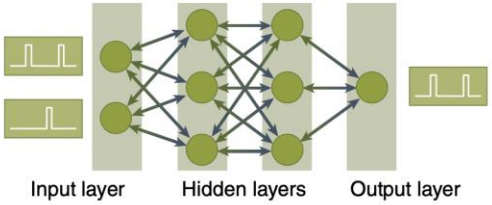
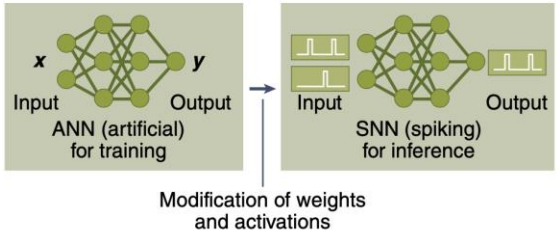
Learning Rules and Training Methods

- Supervised
- Unsupervised
- L2L

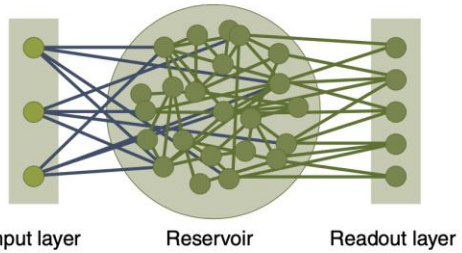
a (Quasi) Backpropagation



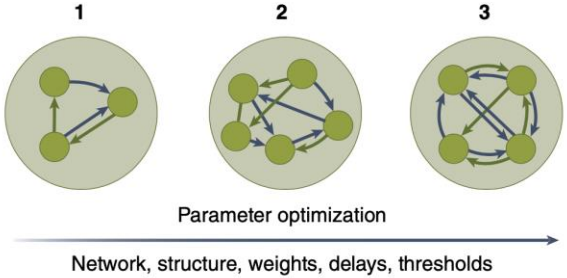
b Mapping Post-training



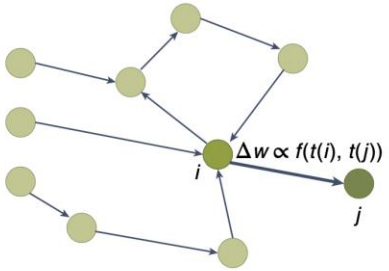
c Reservoir Computing



d Evolutionary Optimisation



e Hebbian Rules, STDP



ALGORITHMS PROS AND CONS

Algorithm Class	Any Model	Device Quirks	Complex to Implement	On-Line	Fast Time to Solution	Demonstrated Broad Applicability	Biologically-Inspired or Plausible
Back-Propagation	No	No	Yes	No	Yes	Yes	No
Evolutionary	Yes	Yes	No	No	No	Yes	Maybe
Hebbian	No	Yes	No	Yes	Maybe	No	Yes
STDP	No	Yes	Maybe	Yes	Maybe	No	Yes

Image sources [15,16]

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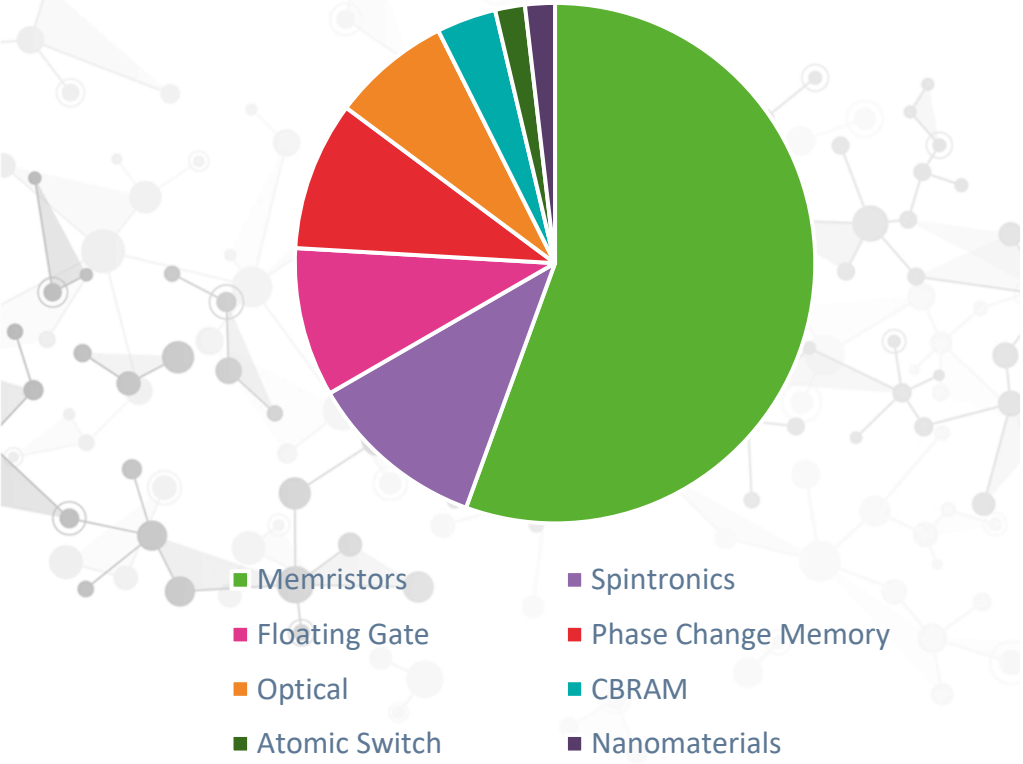
Materials and Technologies



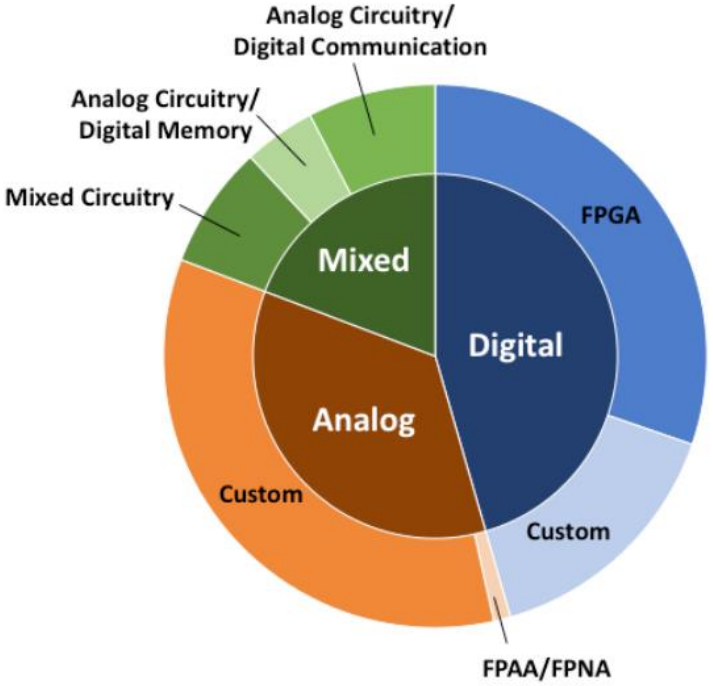


Image source [15], VLSI [40]

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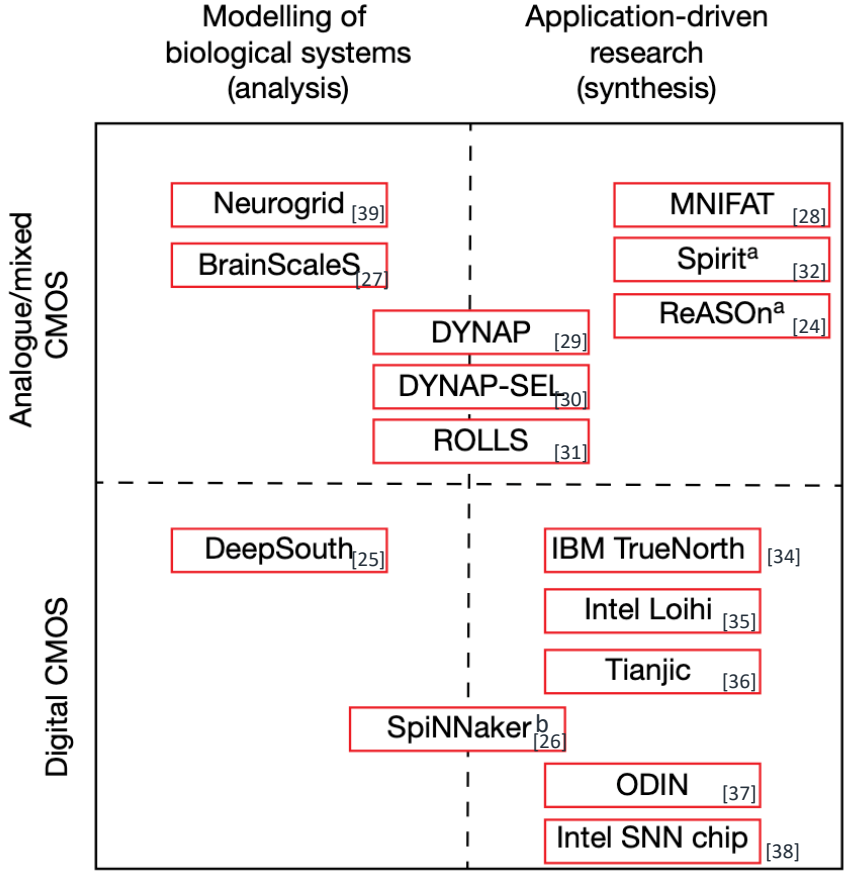
Landscape of Neuromorphic Hardware



Including properties such as:

- In-memory computing
- Fine-grained parallelism
- Learning in hardware
- Event-based and asynchronous communication
- Reduced precision
- Spike-based processing
- Adaptability
- Leveraging noise and stochasticity
- Brain-inspired

a. memristor technology
b. SpiNNaker2 with FP+other features

Image source Mehonic et al. [23]

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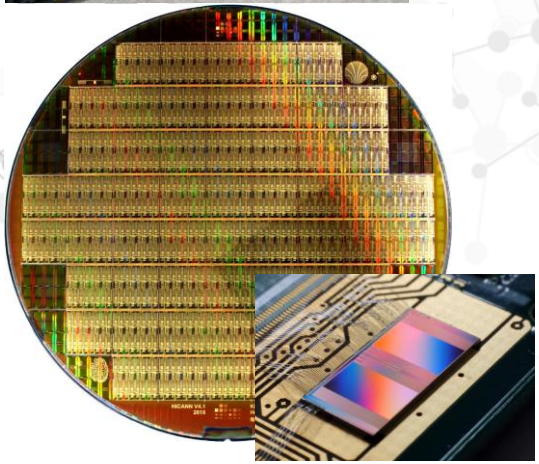
BrainScaleS vs SpiNNaker (HBP)

BrainScaleS

- physical VLSI (analogue or mixed-signal)
- emulations of neuron, synapse and plasticity models
- digital connectivity
- 10,000X times faster than real time



SpiNNaker

- digital multicore chips
- numerical models of neuron, synapse and plasticity on ARM
- custom optimised connectivity
- 10X real time on 1-Mio cores

https://wiki.ebrains.eu/bin/view/Collabs/neuromorphic/

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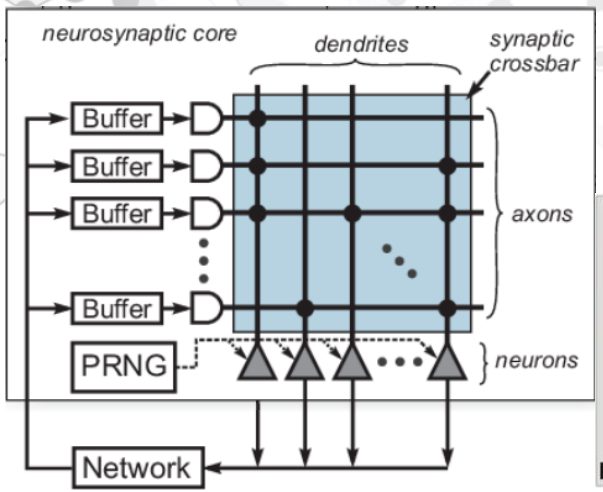
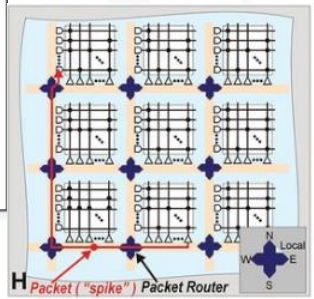
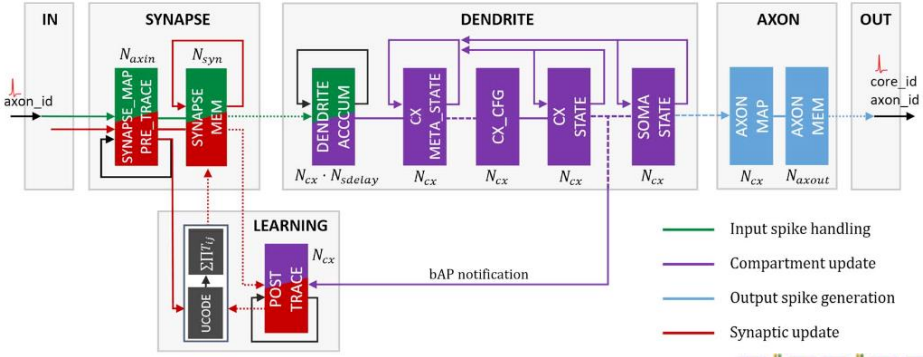
TrueNorth & Loihi

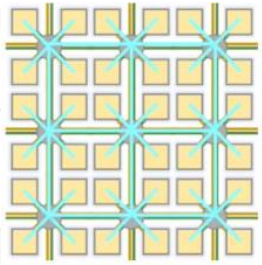
IBM TrueNorth [34,41]

- 4096 Neuro Cores
- Each 256 fully-connected neurons
- 256x256 crossbar (locally synchronous)
- mesh event routing between Neuro Cores (globally asynchronous)
- LIF neurons, multi-valued synapses









Intel Loihi [35]

- 128 Neuromorphic Cores
- Each 1024 primitive neurons
- scalable mesh routing (locally synchronous, globally asynchronous)
- LIF neurons, precision synapses
- Programmable on-chip synaptic learning rules (STDP)
- Programmable synaptic delays

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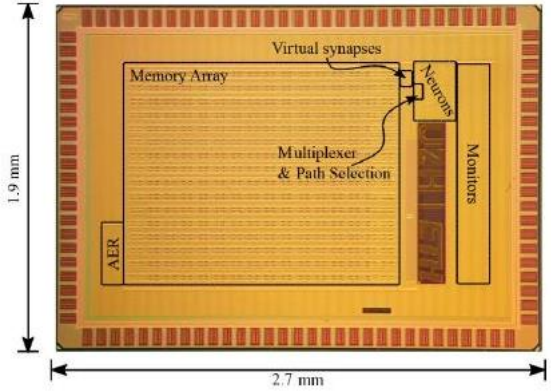
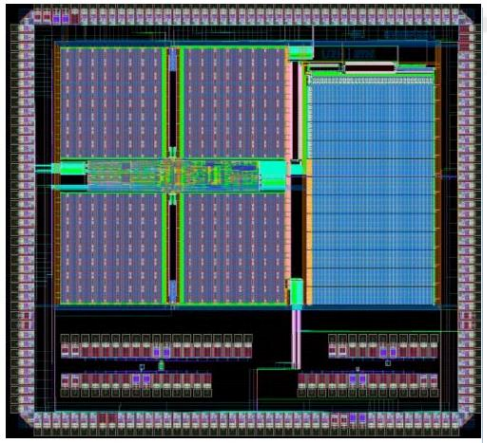
ReASOn / Dynap-sel (28nm FD-SOI) [24]





Block	Number	Detail
Non-Plastic Core	X4	256 X 4 analog AExp Leaky I&F neurons, 16k X4 TCAM-based synapses
Plastic Core	X1	64 analog AExp Leaky I&F neurons, 8k digital plastic synapses 4k digital non-plastic synapses 256 virtual synapses
Neuron		Computation: Pure current based Biological features: NMDA, frequency adaptation, tunable refractory period, firing threshold, fast/slow leaky time constants. Tunable Parameter: 12 biases for Ith, Itau1/2, Idc, Irefr, Imemthr... Local latches for configuration: NMDA, Monitor, tau1/2
Non-plastic Synapse		11-bit TCAM(synapse addresses)+5-bit SRAM (Exc/Inh, 4-bit synaptic weight)
Plastic Synapse		4-bit up/down counter-based digital with Fusi stop learning rule Configurable feature: Exc/Inh, Set weight from 0 to 15, weight monitor enable, Learning Enable/disable, Broadcast event enable/disable

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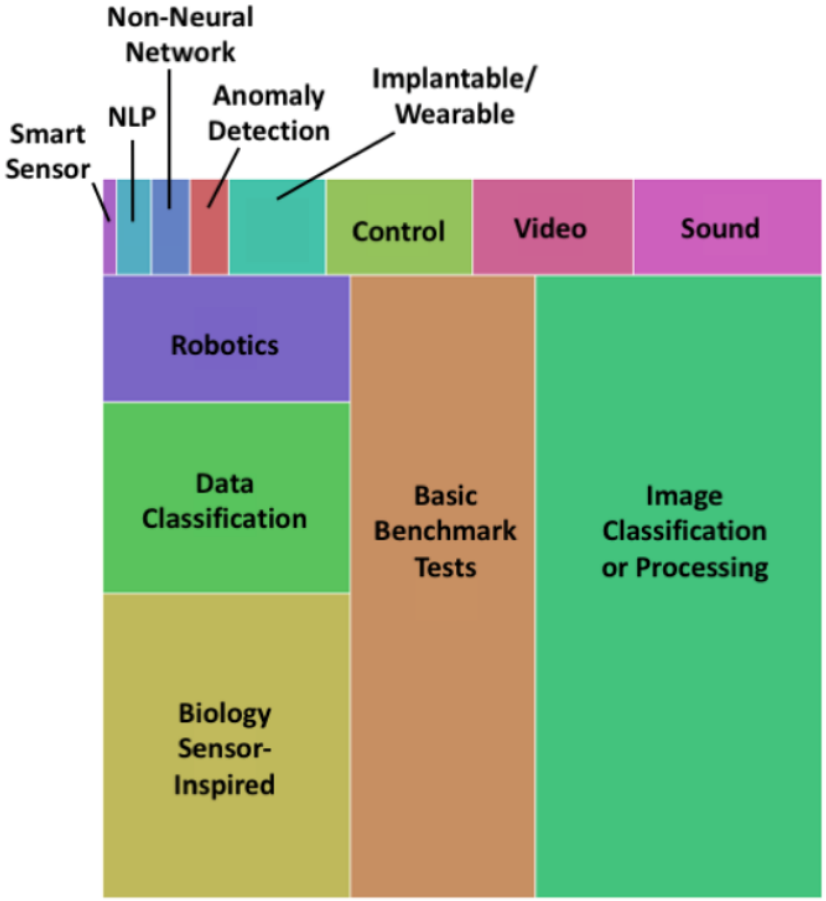
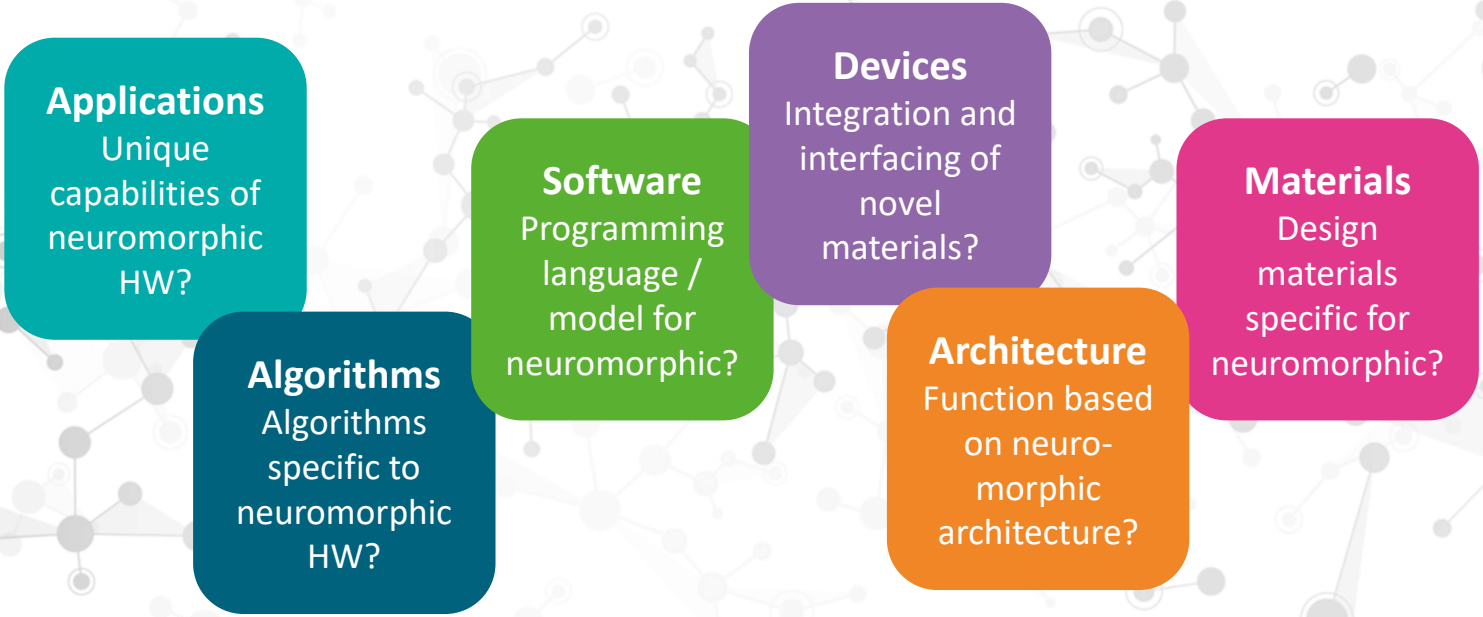
Overview of Applications – Next Talk!



- Data from 2017[15]
- In 2023, probably larger portion of smart sensors and edge AI

Research Areas and Challenges



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